8

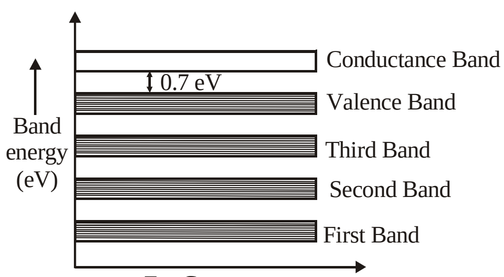
SEMICONDUCTOR & COMMUNICATION SYSTEMS

ENERGY BANDS IN SOLIDS

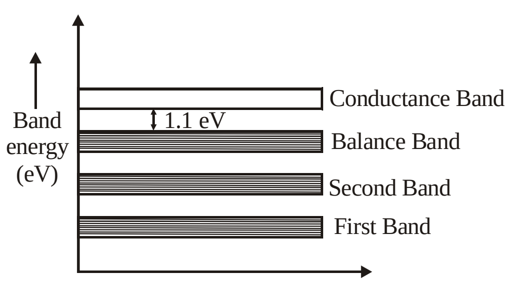
Based on Pauli's exclusion principle

In an isolated atom electrons present in energy level but in solid, atoms are not isolated there is interaction among each other due to this energy level splited into different energy levels. Quantity of these different energy levels depends on the quantity of interacting atoms. Splitting of sharp and closely compact energy levels result into energy band. This is discrete in nature. Order of energy levels in a band is 10^{23} and their energy difference = 10^{-23} eV.

Energy Band : Range of energy possessed by electron in a solid is known as energy band.



For Ge



For Si

Valence Band (VB) : Range of energies possessed by valence electron is known as valence band.

(a) Have bonded electron

(b) No flow of current due to such electron

(c) Always fulfill by electron

Conduction Band (CB) : Range of energies possessed by free electron is known as conduction band.

(a) Also called empty band of minimum energy.

(b) In general partially filled by electron.

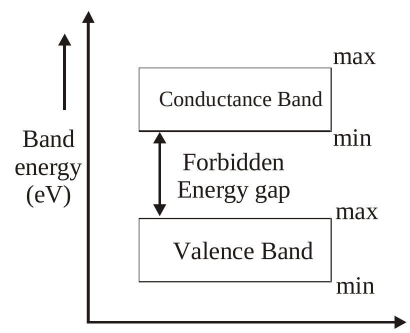
(c) If conduction band is empty, then conduction is not possible.

Forbidden Energy gap (FEG) (aEg)

$$\Delta E_g = (C\,B)_{min} - (V\,B)_{max}$$

* Energy gap between conduction band and valence band, where no free electron can exist.

* Width of forbidden energy gap depends upon the nature of substance.



* Width is more, then valence electrons are strongly attached with nucleus

* Width of forbidden energy gap is represented in eV.

* As temperature increases forbidden energy gap decreases (very slightly).

CLASSIFICATION OF CONDUCTORS, INSULATORS AND SEMICONDUCTOR

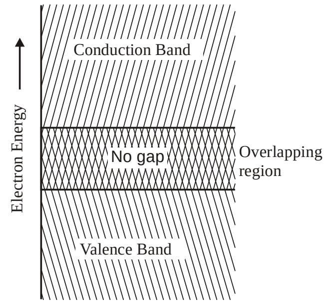
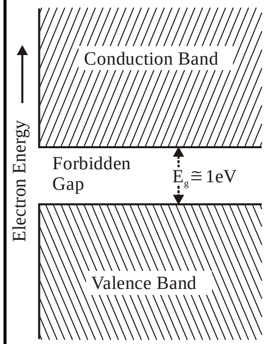
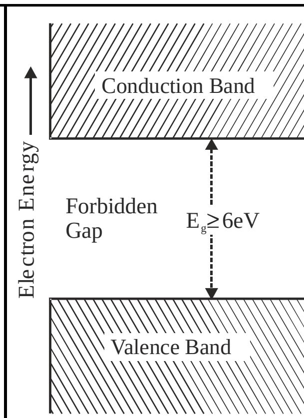
On the basis of the relative values of electrical conductivity and energy bands the solids are broadly classified into three categories

(i) Conductors (ii) Semiconductors

(iii) Insulator

Comparison between conductor, semiconductor and insulator :

Properties	Conductor	Semiconductor	Insulator
Resistivity	$10^{-2} - 10^{-8}\ \Omega m$	$10^{-5} - 10^{6}\ \Omega m$	$10^{11} - 10^{19}\ \Omega m$
Conductivity	$10^{2} - 10^{8}$ mho/m	$10^{5} - 10^{-6}$ mho/m	$10^{-11} - 10^{-19}$ mho/m
Temp. Coefficient of resistance (α)	Positive	Negative	Negative
Current	Due to free electrons	Due to electrons and holes	No current

Energy band diagram	 Conductor	 Semiconductor	 Insulator
Forbidden energy gap	$\cong$ 0eV	$\cong$ 0 – eV	$\geq$ 6eV
Example	Pt, Al, Cu, Ag	Ge, Si, C, GaAs GaF_2	Wood, plastic Diamond, Mica

EFFECT OF TEMPERATURE

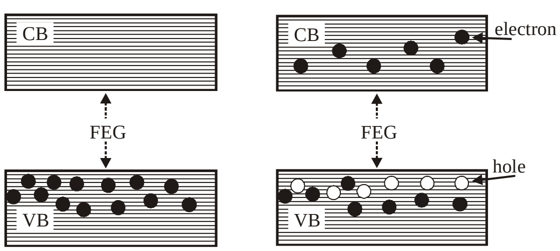
At absolute zero kelvin temperature :

At this temperature covalent bonds are very strong and there are no free electrons and semiconductor behaves as perfect insulator.

Above absolute temperature : With increase in temperature some covalent bonds are broken and few valence electrons jump to conduction band and hence it behave as poor conductor.

CONCEPT OF HOLES IN SEMICONDUCTORS

Due to external energy (temp. or radiation) when electron goes from valence band to conduction band (i.e. bonded electrons becomes free), vacancy of free e^- create in valence band, which has same charge as electron but positive. This positively charged. Known as hole and shown in figure. It is deficiency of electron in VB. It acts as positive charge. It's effective mass is more than electron. It's mobility of hole is less than electron. Hole acts as virtual charge, although there is no physical charge on it.



Pure semiconductor At 0 K temp.   Pure semiconductor At room temp.

Hole Current: At room temperature, due to breaking of some Covalent bonds some free electrons are produced. By applying electric field current flow due to free electrons and hole current also flow in semiconductor.

EFFECT OF IMPURITY IN SEMICONDUCTOR

Doping is a method of addition of desirable impurity atoms to pure semiconductor to increase conductivity of semiconductor.

Doping is a process of deliberate addition of a desirable impurity atoms to a pure semiconductor to modify its properties in controlled manner.

Added impurity atoms are called dopants.

The impurity added may be $\approx$ 1 part per million (ppm).

* The dopant atom should take the position of semiconductor atom in the lattice.
* The presence of the dopant atom should not distort the crystal lattice.
* The size of the dopant atom should be almost the same as that of the crystal atom.
* The concentration of dopant atoms should not be large (not more than 1% of the crystal atom).

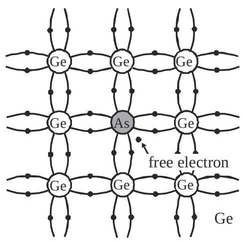
It is to be noted that the doping of a semiconductor increases its electrical conductivity to a great extent.

METHODS OF DOPING

1. Add the impurity atoms in the molten semiconductor.
2. Heat the crystalline semiconductor in an atmosphere containing dopant atoms or molecules so that the latter diffuse into the semiconductor.
3. Implant dopant atoms by bombarding the semiconductor with their ions.

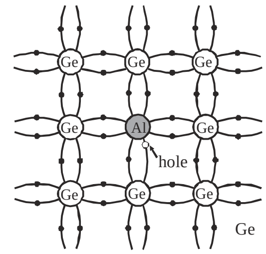
N TYPE SEMICONDUCTOR

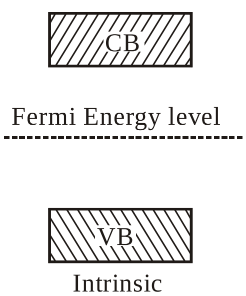
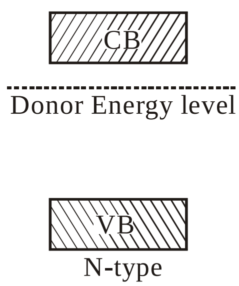
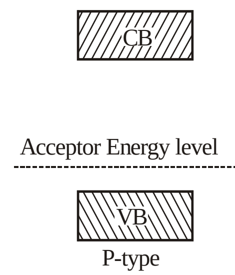
When a pure semiconductor (Si or Ge) is doped by pentavalent impurity (P, As, Sb, Bi) then four electrons out of the five valence electrons of impurity take part, in covalent bonding, with four silicon atoms surrounding it and the fifth electron is set free. These impurity atoms which donate free e^- for conduction are called as Donor impurity (N_D). Here free e^- increases very much so it is called as N type semiconductor. Here impurity ions known as “Immobile Donor positive Ion”. Free e^- called as majority charge carriers and holes called as minority charge carriers.



P TYPE SEMICONDUCTOR

When a pure semiconductor (Si or Ge) is doped by trivalent impurity (B, Al, In, Ga) then outer most three electrons of the valence band of impurity take part, in covalent bonding with four silicon atoms surrounding it and except one electron from semiconductor and make hole in semiconductor. These impurity atoms which accept bonded e^- from valance band are called as Acceptor impurity (N_A). Here holes increases very much so it is called as P type semiconductor here impurity ions known as “Immobile Acceptor negative Ion”. Free e^- are called as minority charge carries and holes are called as majority charge carriers.



Intrinsic Semiconductor	N-type (Pentavalent impurity)	P-type(Trivalent impurity)
1. 		
2. Current due to electron and hole	Mainly due to electrons	Mainly due to holes
3. $n_e = n_h = n_1$	$n_h << n_e$ ($N_D \simeq n_e$)	$n_h >> n_e$ ($N \simeq n$)
4. $I = I_e + I_n$	$I \simeq I_e$	$I \simeq I_h$
5. Entirely neutral	Entirely neutral	Entirely neutral
6. Quantity of electrons and holes are equal	Majority - Electrons Minority - Holes	Majority - Holes Minority - Electrons

MASS ACTION LAW

* The electron and hole concentration in a semiconductor in thermal equilibrium is given by : $n_e n_h = n_i^2$
where, n_i is density of electrons or holes in a pure semiconductor and is called intrinsic concentration.

RESISTIVITY AND CONDUCTIVITY OF SEMICONDUCTOR

Conduction in conductor :

* Relation between current (I) and drift velocity (v_d)
$I = neAv_d$,
n = number of electron in unit volume,
A= cross sectional area

* Current density, $J = I / A = ne\, v_d$

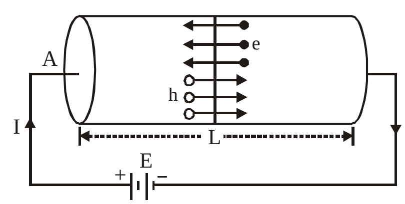
* Drift velocity of electron $v_d = \mu E$

* Mobility $\mu = v_d/E$

* $J = ne\,\mu E$; $J = \sigma E$

* Conductivity, $\sigma = ne\mu = 1/\rho$
ρ = Resistivity

Conduction in semiconductor



Intrinsic semiconductor	P-Type	N-Type
$n_e = n_h$ $J = n_e[v_e+v_h]$ $\sigma = 1/\rho$ $= en\,[\mu_e+\mu_h]$	$n_h >> n_e$ $J \cong e\, n_h\, v_h$ $\sigma = 1/\rho$ $\cong e\, n_h\, \mu_h$	$n_e >> n_h$ $J \cong e\, n_e\, v_e$ $\sigma = 1/\rho$ $\cong e\, n_e\, \mu_e$

Example 1 :

The energy of a photon of sodium light (λ = 589 nm) equals the band gap of a semiconducting material. Find:

(a) the minimum energy E required to create a hole-electron pair.

(b) the value of (E/kT)at a temperature of 300 K.

Sol. (a) $E = \frac{hc}{e\lambda}$ (in eV). So, $E = \frac{12400}{\lambda}$ (E is eV and λ is in Å)

$$\text{So, } E = \frac{12400}{5890} = 2.1 \text{ eV}$$

(b) $$\frac{E}{kT} = \frac{2.1 \times 1.6 \times 10^{-19} \text{ J}}{1.38 \times 10^{-23} \times 300} = 81$$

Example 2 :

A P type semiconductor has acceptor level 57 meV above the valence band. What is maximum wavelength of light required to create a hole ?

Sol. $$E = \frac{hc}{\lambda} \Rightarrow \lambda = \frac{hc}{E} = \frac{6.62 \times 10^{-34} \times 3 \times 10^{8}}{57 \times 10^{-3} \times 1.6 \times 10^{-19}} = 217100 \text{ Å}$$

Example 3 :

What will be the conductance of pure silicon crystal at 300K temp. If electron hole pairs per cm^3 is 1.072×10^{10} at this temp., μ_n = 1350 cm^2/volt sec and μ_p = 480cm^2/volt sec.

Sol. $\sigma = n_i e\mu_e + n_i e\mu_h = n_i e(\mu_e + \mu_h) = 3.14 \times 10^{-6}$ mho/cm

P-N JUNCTION

Techniques for making P-N junction

Alloy Junction : Here a small piece of III group impurity like indium is placed over n-Ge or n-Si and melted ultimately P-N junction form.

Diffusion Junction : A heated P-type semiconductor is kept in pentavalent impurity vapours which diffuse into P-type semiconductor and make P-N junction.

Vapour deposited junction or epitaxial junction

If we want to grow a layer of n-Si or p-Si then p-Si wafer is kept in an atmosphere of Silane (a silicon compound which dissociates into Si at high temperatures) plus phosphorous vapours.

On crackling of silane at high temperature a fresh layer on n-Si grows on p-Si giving the P-N junction.

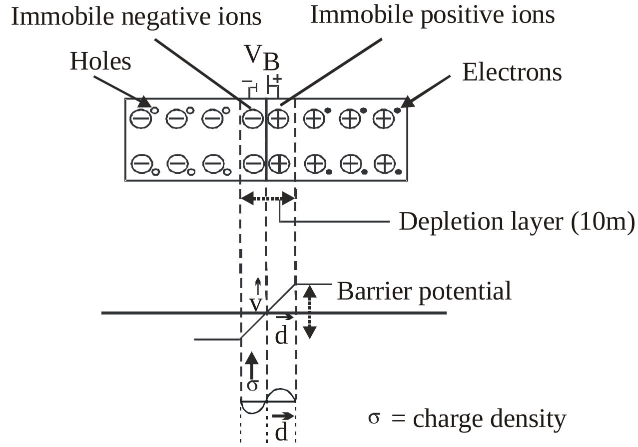
Since this junction growth is layer by so it is also referred as layer growth or epitaxial junction formation of P-N junction.

Description of P-N Junction without applied voltage or bias A P-N junction immediately after it is formed has P region with mobile majority holes and immobile negatively charged impurity ions.

N region has mobile majority free electrons and immobile positively charged impurity ions.

Due to concentration difference diffusion of holes starts from P to N side and diffusion of e^- s starts N to P side.

Due to this a layer of only positive (in N side) and negative (in P-side) started to form which generate an electric field (N to P side) which oppose diffusion process, during diffusion magnitude of electric field increases due to this diffusion it gradually decreased and ultimately stops.



The layer of immobile positive and negative ions, which have no free electrons and holes called as depletion layer.

Diffusion and drift current :

(1) Diffusion current - P to N side

(2) Drift current - N to P side

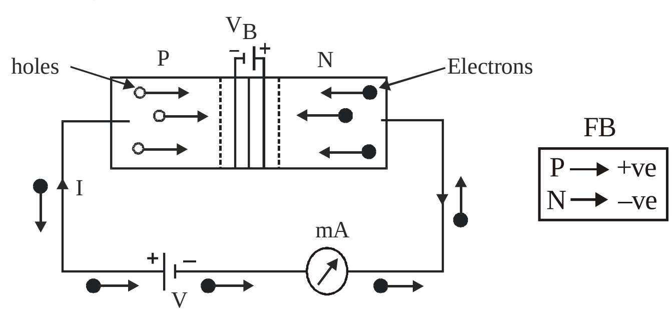
If there is no biasing diffusion current = drift current

So total current is zero

Behaviour of P-N junction with an external voltage applied or bias :

Forward Bias : If we apply a voltage V such that P-side is positive and N-side is negative as shown in diagram.

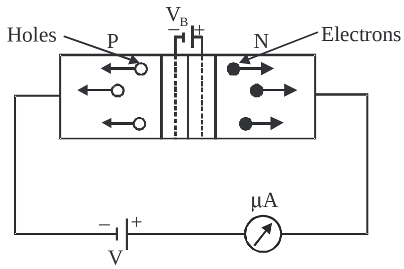
The applied voltage is opposite to the junction barrier potential. Due to this effective potential barrier decreases, junction width also decreases, so more majority carriers will be allowed to flow across junction. It means the current flow in principally due to majority charge carries and is large (mA) called as forward Bias.



Reverse Bias : If we apply a voltage V such that P-side is negative and N-side is positive as shown in diagram.

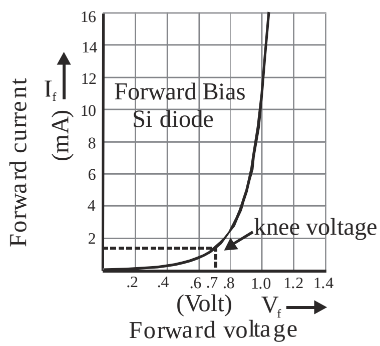
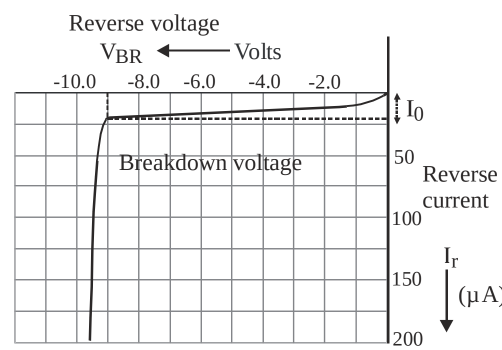
The applied voltage is same side to the junction barrier potential. Due to this effective potential barrier increased junction width also increased, so no majority carriers will be allowed to flow across junction.

Only minority carriers will drifted. It means the current flow in principally due to minority charge carries and is very small (μA) called as reversed Bias.



RB

P → –ve
N → +ve

Forward bias	Reverse Bias
1. Potential Barrier reduces	1. Potential Barrier increases.
2. Width of depletion layer decrease	2. Width of depletion layer increases.
3. P-N Jn Provide very small resistance	3. P-N Jn. Provide high resistance
4. Forward current flow in circuit	4. Very small current flow.
5. Order of forward current in milli amp.	5. Order of current in micro amp. (Ge) or Neno amp. (Si).
6. Mainly flow majority current flows.	6. Mainly minority current flows
7. Forward characteristic curves. 	7. Reverse characteristic curve 
8. Forward resistance	8. Reverse resistance
$R_f = \dfrac{\Delta V_f}{\Delta I_f} \cong 100\,\Omega$	$R_B = \dfrac{\Delta V_B}{\Delta I_B} \cong 10^6\,\Omega$
9. Knee or cut in voltage	9. Breakdown voltage
$Ge \to 0.3\,V,\ Si \to 0.7\,V$	$Ge \to 25\,V,\ Si \to 35\,V$

Note : $\dfrac{R_B}{R_F} = 10^3 : 1$ for Ge ; $\dfrac{R_B}{R_F} = 10^4 : 1$ for Si

Example 4 :

A zener diode of voltage V_Z (= 6V) is used to maintain a constant voltage across a load resistance R_L (= 1000 Ω) by using a series resistance R_s (=100Ω). If the e.m.f. of source is E (= 9 V), calculate the value of current through series resistance, Zener diode and load resistance. What is the power being dissipated in Zener diode.

Sol. Here, $E = 9V;\ V_z = 6;\ R_L = 1000\Omega$ and $R_s = 100\Omega$,

Potential drop across series resistor

$v = E - V_Z = 9 - 6 = 3V$

Current through series resistance R_S is

$$I = \frac{V}{R} = \frac{3}{100} = 0.03\,A$$

Current through load resistance R_L is

$$I_L = \frac{V_Z}{R_L} = \frac{6}{1000} = 0.006\,A$$

Current through Zener diode is

$I_Z = I - I_L = 0.03 - 0.006 = 0.024$ amp.

Power dissipated in Zener diode is

$P_Z = V_Z I_Z = 6 \times 0.024 = 0.144$ Watt

Example 5 :

A Zener diode is specified having a breakdown voltage of 9.1V with a maximum power dissipation of 364 mW. What is the maximum current that the diode can handle.

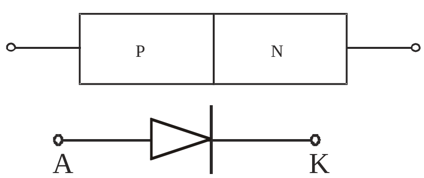
Sol. Maximum current that the given diode can handle is

$$= \frac{364 \times 10^{-3}}{9.1} = 40\text{ mA.}$$

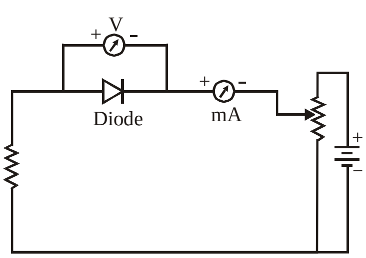
REVERSE BREAK DOWN

* If the reverse bias voltage is made too high, the current through the PN junction increases rapidly at V_Z . The voltage at which this happens is called **breakdown voltage** or Zener voltage.
* There are two mechanism which causes this breakdown. One is called Zener breakdown and the other is called avalanche breakdown.
* **Zener breakdown :** When reverse bias is increased the electric field at the junction also increases. At some stage the electric field becomes so high that it breaks the covalent bonds creating electron, hole pairs. Thus a large number of carriers are generated. This causes a large current to flow. This mechanism is known as Zener breakdown.
* **Avalanche breakdown :** At high reverse voltage, due to high electric field, the miniority charge carriers, while crossing the junction acquires very high velocities. These by collision breaks down the covalent bonds, generating more carriers. A chain reaction-is established, giving rise to high current. This mechanism is called avalanche breakdown.

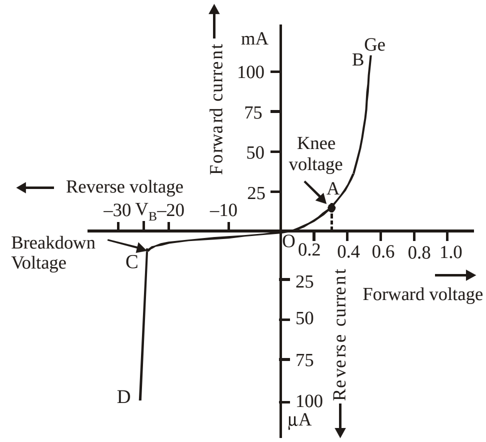
CHARACTERISTIC CURVE OF P-N JUNCTION DIODE



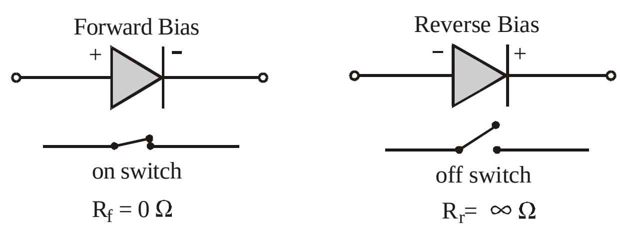
In forward bias when voltage is increased from 0V in steps and corresponding value of current is measured, the curve comes as OB of figure. We may note that current increase very sharply after a certain voltage knee voltage. At this voltage, barrier potential is completely eliminated and diode offers a low resistance.



In reverse bias a microammeter has been used as current is very very small. When reverse voltage is increased from 0V and corresponding values of current measured the plot comes as OCD. We may note that reverse current is almost constant hence called reverse saturation current. It implies that diode resistance is very high. As reverse voltage reaches value V_B, called breakdown voltage, current increases very sharply.



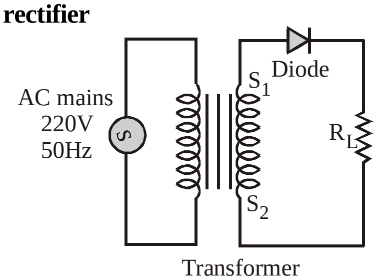
For Ideal Diode

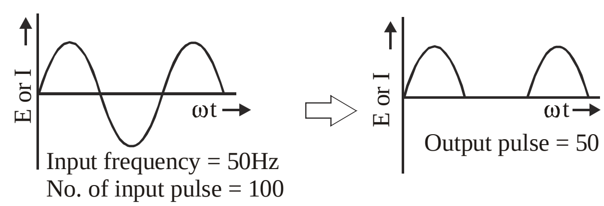


RECTIFIER

It is device which is used for converting alternating current into direct current.

Half wave rectifier





During the first half (positive) of the input signal. Let S_1 is at positive and S_2 is at negative potential. So, the PN junction diode D is forward biased. The current flows through the load resistance R_L & output voltage is obtained. During the second half (negative) of the input signal, S_1 and S_2 would be negative and positive respectively. The PN junction diode will be reversed biased. In this case, practically no current would flow through the load resistance. So, there will be no output voltage.

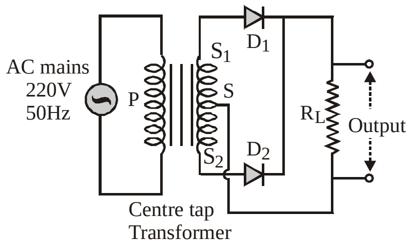
Thus, corresponding to an alternating input signal, we get a unidirectional pulsating output.

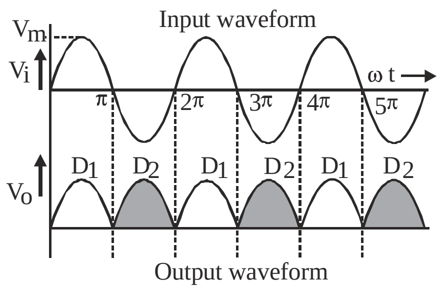
Peak voltage (PIV) $V_s = V_{in}$

In half wave rectifier PIV = maximum voltage across secondary coil of transformer.

Full wave rectifier

When the diode rectifies the whole of the AC wave, it is called full wave rectifier. Figure shows the experimental arrangement for using diode as full wave rectifier. The alternating signal is fed to the primary a transformer. The output signal appears across the load resistance R_L.





During the positive half of the input signal :

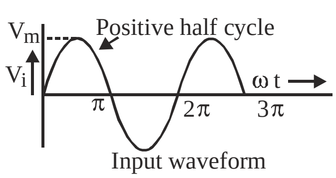
Let S_1 positive and S_2 negative.

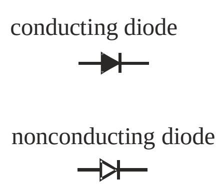
In this case diode D_1 is forward biased and D_2 is reverse biased. So only D_1 conducts and hence the flow of current in the load resistance R_L is from A to B.

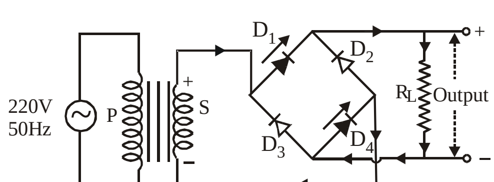
During the negative half of the input signal :

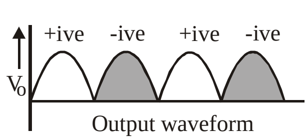
Now S_1 is negative and S_2 is positive. So D_1 is reverse-biased and D_2 is forward biased. So only D_2 conducts and hence the current flows through the load resistance R_L from A to B. It is clear that whether the input signal is positive or negative, the current always flows through the load resistance in the same direction and full wave rectification is obtained.

Bridge Rectifier :









During positive half cycle

D_1 and D_4 are forward biased → on switch

D_2 and D_3 are reverse biased → off switch

During negative half cycle

D_2 and D_3 are forward biased → on switch

D_1 and D_4 are reverse biased → off switch

In bridge rectifier peak inverse voltage

$$PIV = V_s = V_m$$

Form Factor : $F = \dfrac{I_{rms}}{I_{dc}}$ or $\dfrac{E_{rms}}{E_{dc}}$

For full wave rectifier $F = \dfrac{\pi}{2\sqrt{2}}$

for half wave rectifier $F = \pi/2$

Ripple and ripple factor : In the output of rectifier some A. C. components are present. They are called ripple & there measurement is given by a factor so it is called ripple factor. For good rectifier ripple factor must be very low.

Total output current

Where $I_{rms} = \sqrt{I_{ac}^2 + I_{dc}^2}$

I_{ac} = rms value of AC component

Ripple factor $= r = \dfrac{I_{ac}}{I_{dc}} \quad \Rightarrow r = \sqrt{\dfrac{I_{rms}^2}{I_{dc}^2} - 1} = \sqrt{F^2 - 1}$

Rectifier efficiency $\quad \eta = \dfrac{P_{dc}}{P_{ac}} = \dfrac{I_{dc}^2 R_L}{I_{rms}^2 (R_F + R_L)}$

Half wave rectifier	**Full wave rectifier or bridge wave rectifier**
$\eta = \dfrac{0.406}{1 + \dfrac{R_f}{R_L}}$ if $\dfrac{R_f}{R_L} << 1$	$\eta = \dfrac{0.812}{1 + \dfrac{R_f}{R_L}}$ if $\dfrac{R_f}{R_L} << 1$
$\eta = 40.6\%$	$\eta = 81.2\%$
If $R_f = R_L$	If $R_f = R_L$
$\eta = 20.3\%$	$\eta = 40.6\%$
	In bridge full wave rectifier R_f is two times of resistance of P-N in FB

FILTERS

* Filter circuits smooth out the fluctuations in amplitude or ac ripple of the output voltage obtained from a rectifier.

* Filter circuit consists of capacitor or/and choke coils.

* A capacitor offers a high resistance to low frequency AC ripple (infinite resistance to DC) and a low resistance to high frequency AC ripple. Therefore, it is always used as a shunt to the load.

* A choke coil offers high resistance to high frequency AC, and almost zero resistance to DC. It is used in series.

Example 6 :

A sinusoidal voltage of amplitude 25 volts and frequency 50Hz is applied to a half wave rectifier using PN diode. No filter is used and the load resistor is 1000Ω. The forward resistance R_f ideal diode is 10Ω. Calculate

(i) Peak, average and rms values of load current.

(ii) d.c. power output (iii) a.c. power input

(iv) % Rectifier efficiency (v) Ripple factor

Sol. (i) $I_m = \dfrac{V_m}{R_f + R_L} = \dfrac{25}{(10+1000)} = 24.75\text{ mA}$

$$I_{dc} = \frac{I_m}{\pi} = \frac{24.75}{3.14} = 7.87\text{ mA} ; \ I_{rms} = \frac{I_m}{2} = \frac{24.75}{2} = 12.37\text{ mA}$$

(ii) $P_{dc} = I_{dc}^2 \times R_L = (7.87 \times 10^{-3})^2 \times 10^3 = 61.9\text{ mW}$

(iii) $P_{ac} = I_{rms}^{\ 2}(R_f + R_L) = (12.37 \times 10^{-3})^2 \times (10 + 1000)$
$= 154.54\text{ mW}$

(iv) Rectifier efficiency

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100 = \frac{61.9}{154.54} \times 100 = 40.05\%$$

$$\text{(v) Ripple factor} = \left[\left(\frac{I_{rms}}{I_{ac}}\right)^2 - 1\right]^{1/2} = \left[\left(\frac{12.37}{7.87}\right)^2 - 1\right] = 1.21$$

Example 7 :

The halfwave rectifier supplies power to a 1kΩ load, The input supply voltage is 220 V neglecting forward resistance of the diode, calculate (i) V_{dc} (ii) I_{dc} and (iii) Ripple voltage (rms value).

Sol. (i) $V_{dc} = \dfrac{V_m}{\pi} = \dfrac{\sqrt{2}\ V_{rms}}{2} = \dfrac{\sqrt{2} \times 220}{3.14} = 98.79\text{ V}$

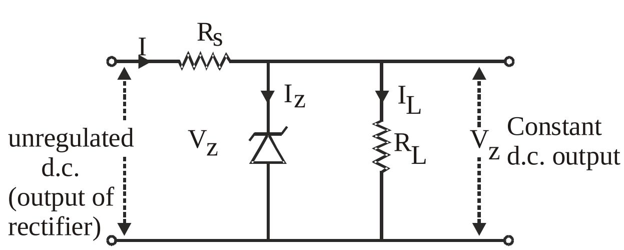
(ii) $I_{dc} = \dfrac{V_{dc}}{R_L} = \dfrac{98.79}{1000} = 98.79\text{ mA}$

(iii) $r = \dfrac{(V_r)_{rms}}{V_{dc}}$ or $(V_r)_{rms} = r \times v_{dc}$

$(V_r)_{rms} = r \times v_{dc} = 1.21 \times 98.79 = 119.53\text{ V}$

ZENER DIODE

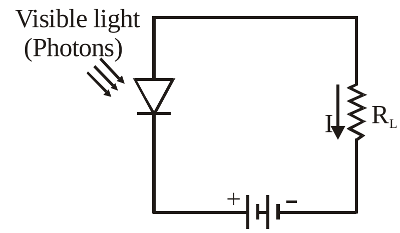
A properly doped crystal diode which has sharp break down voltage is known as Zener diode. It is always connected in reverse biased condition manner. Used as a voltage regulator.



In forward biased it works as a simple diode.

SOME SPECIAL DIODES

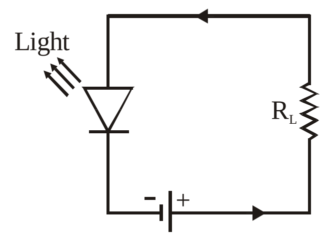
Photodiode : A junction diode made from light or photo sensitive semiconductor is called a photo diode.



When light of energy "hνν" falls on the photodiode (Here hν > energy gap) more electrons move from valence band, to conduction band, due to this current in circuit of photodiode in "Reverse bias", increases. As light intensity is increased, the current goes on increases so photo diode is used, "to detect light intensity" for example it is used in "Video camera".

Light emitting diode (L.E.D) : When a junction diode is "forward biased" energy is released at junction in the form of light due to recombination of electrons and holes. In case of Si or Ge diodes, the energy released is in infra-red region.

In the junction diode made of GaAs, InP etc. energy is released in visible region such a junction diode is called "light emitting diode" (LED)



Solar cell : Solar cell is a device for converting solar energy into electrical. A junction diode in which one of the P or N sections is made very thin (So that the light energy falling on diode is not greatly absorbed before reaching the junction) can be used to convert light energy into electric energy such diode called as solar cell.

(i) It is operated into photo voltaic mode i.e., generation of voltage due to the bombardment of optical photon.

(ii) No external bias is applied.

(iii) Active junction area is kept large, because we are intrested in more power. Materials most commonly used for solar cell is Si, As, Cds, CdTe, CdSe, etc.

Variable capacitor (Varactor)

P - N junction diode can be used as a "Capacitor" here depletion layer acts as "dielectric material" and remaining P and N part acts as metallic plates.

Diode laser : It is interesting form of LED in which special construction helps to produce stimulated radiation as in laser.

Example 8 :

A potential barrier of 0.5 V exists across a p-n junction (i) If the depletion region is 5×10^{-7} m wide. What is the intensity of the electric field in this region? (ii) An electron with speed 5×10^5 m/s approaches the p-n junction from the n-side with what speed it will enter the p-side.

Sol. (i) Width of depletion layer $\Delta L = 5 \times 10^{-7}$ m

$$E = \frac{V}{\Delta L} = \frac{0.5V}{5\times10^{-7}} = 10^6 \text{ volt/m}$$

(ii) Work energy theorem, $\frac{1}{2}Mv_i^2 = eV + \frac{1}{2}Mv_f^2$

$$v_f = \sqrt{\frac{Mv_i^2 - 2eV}{M}} = 2.7 \times 10^5 \text{ m/s}$$

TRANSISTOR

Inventor William Bradford Shockley, John Bardeen and Walter Houser Brattain.

Transistor is a three terminal device which transfers a signal from low resistance circuit to high resistance circuit. It is formed when a thin layer of one type of extrinsic semiconductor P or N type is sandwitched between two thick layers of other two type extrinsic semiconductor.

Each transistor have three terminals which are :

(i) Emitter (ii) Base (iii) Collector

Emitter : It is the left most part of the transistor. It emit the majority carrier towards base. It is highly doped and medium in size.

Base : It is the middle part of transistor which is sandwitched by emitter (E) and collector (C). It is lightly doped and very thin in size.

Collector : It is right part of the transistor which collect the majority carrier which is emitted by emitter. It have large size and moderately doped.

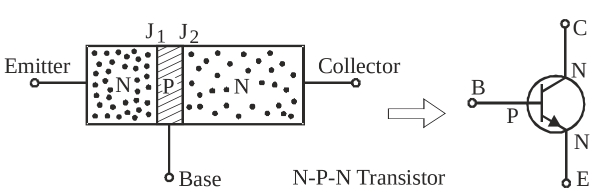
There are two semiconductor junction in transistor

(i) The junction between emitter and base is known as emitter-base junction (J_{EB}).

(ii) The junction between base and collector is known as base-collector junction (J_{CB}).

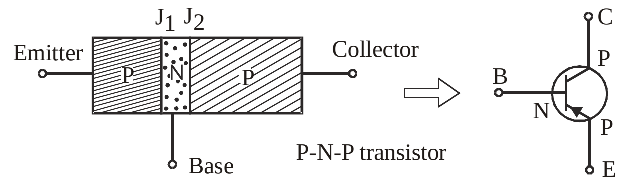
TRANSISTOR ARE OF TWO TYPES

N-P-N Transistor : If a thin layer of P-type semiconductor is sandwitched between two thick layers of N-type semiconductor is known as NPN transistor.



N-P-N Transistor

P-N-P Transistor : If a thin layer of N-type of semiconductor is sandwitched between two thick layer of P-type semiconductor is known as PNP transistor.



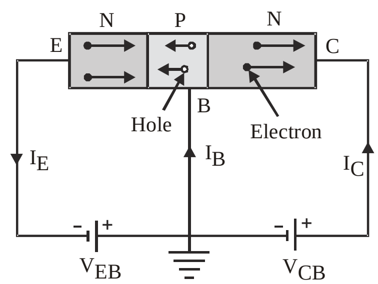
P-N-P transistor

* **Transistor action :** There are four possible ways of biasing the two PN junctions (emitter junction and collector junction) of a transistor. These are tabulated below.

Emitter junction bias	Collector junction bias	Transistor operation
Forward	Reverse	Active
Forward	Forward	Saturation
Reverse	Reverse	Cut off
Reverse	Forward	inverted

A transistor is mostly used in the active region of operation, i.e., the emitter juction is forward biased and the collector junction is reverse biased.

WORKING OF NPN TRANSISTOR



When emitter base junction is forward bias, electrons (majority carriers) in emitter are repelled toward base. The barrier of emitter base junction is reduced and the electron enter the base, about 5% of these electron recombine with hole in base region result in small current (I_b).

The remaining electron (95%) enter the collector region because they are attracted towards the positive terminal of battery.

For each electron entering the positive terminal of the battery is connected with collector base junction an electron from negative terminal of the battery connected with emitter base junction enters the region.

The emitter current (I_e) is more than the collector (I_c).

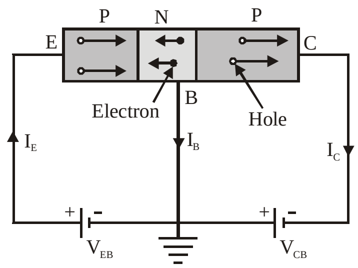
The base current is the difference between Ie and I_c and proportional to the number of electron hole recombination in the base. In above process,

$I_e = I_b + I_c$ is maintained.

WORKING OF PNP TRANSISTOR

When emitter-base junction is forward biased holes (majority carriers) in the emitter are repelled towards the base and diffuse through the emitter base junction. The barrier potential of emitter-base junction decreases and hole enter the n-region (i.e. base). A small number of holes (≈ 5%)

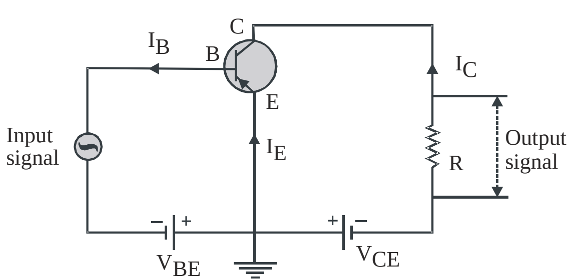
combine with electron of base-region resulting small current (I_b). The remaining hole (≈ 95%) enter into the collector region because they are attracted towards negative terminal of the battery connected with the collector-base junction. These hole constitute the collector current (I_c).



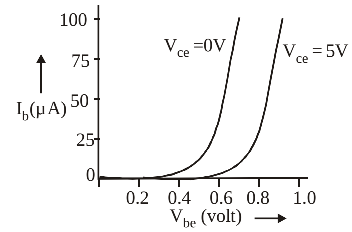
As one hole reaches the collector, it is neutralized by the battery. As soon as one electron and a hole is neutralized in collector a covalent bond is broken in emitter region. The electron hole pair is produced. The released electron enter the positive terminal of battery and hole more towards the collector. In above process, $I_e = I_b + I_c$ is maintained.

Basic Transistor Circuit Configurations :
To study about the characteristics of transistor we have to make a circuit [In which four terminals are required. But the transistor have three terminals, so keeping one of the terminal of transistor as common in input and output both, We have three possible configuration of transistor circuit.
(i) Common base configuration
(ii) Common emitter
(iii) Common collector
In these three common emitter is widely used and common collector is rarely used.

Common emitter characteristic of a transistor
Input characteristics : The variation of base current (I_b) (input) with base emitter voltage (V_{BE}) at constant-emitter voltage (V_{CE}) is called input characteristic.

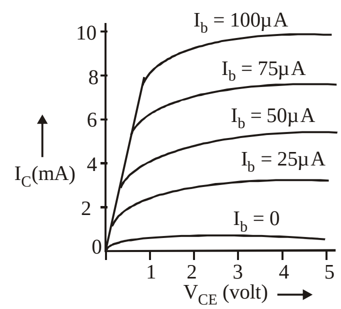


(i) Keep the collector-emitter voltage (V_{CE}) constant (say $V_{CE} = 1V$)
(ii) Now change emitter base voltage and note the corresponding value of base current (I_b).
(iii) Plot the graph between V_{EB} and I_b.



(iv) A set of such curves can be plotted at different V_{CE}

Output characteristics :
The variation of collector current I_c (output) with collector-emitter voltage (V_{CE}) at constant base current (I_b) is called output characteristic.
(i) Keep the base current (I_b) constant (say $I_b = 10\mu A$)
(ii) Now change the collector-emitter voltage (V_{CE}) and note the corresponding values of collector current (I_c).
(iii) Plot the graph between (V_{CE} versus I)



(iv) A set of such curves can be plotted at different fixed values of base current (say 0, 20 μA, 30 μA etc.)

PARAMETERS OF TRANSISTORS

* From linear segments of both the input and output characteristics ac parameters of transistors can be calculated.

Input resistance (r_i):

* The ratio of change in base emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}).

* This is a dynamic ac resistance. $r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}}$

Output resistance (r_o):

* The ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at a constant base current I_B. $r_o = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$

* The reciprocal of the slope of the linear part of the output characteristic gives the values of r_o.

* The output resistance of the transistor is mainly controlled by the bias of the basecollector junction.

* The high magnitude of the output resistance (of the order of 100 kΩ) is due to the reverse-biased state of this diode.

* When the transistor is in saturation state, resistance is very low.

Current amplification factor ( ):

* The ratio of the change in collector current to the change in base current at a constant collector-emitter voltage (V_{CE}) when the transistor is in active state.

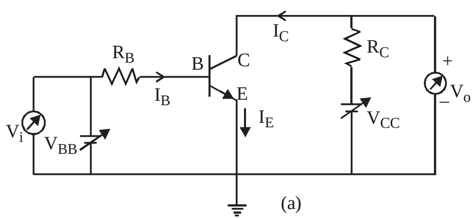
$$\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

* This is also known as small signal current gain and its value is very large.
* If we simply find the ratio of I_C and I_B we get what is called dc β of the transistor. Hence, $\beta_{dc} = \frac{I_C}{I_B}$

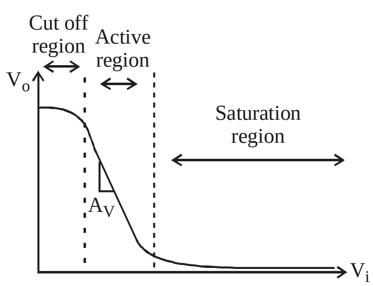
  Since I_C increases with I_B almost linearly and $I_C = 0$ when $I_B = 0$, the values of both β_{dc} and β_{ac} are nearly equal. So, for most calculations β_{dc} can be used.
* Both β_{ac} and β_{dc} vary with V_{CE} and I_B (or I_C) slightly.

TRANSISTOR AS A SWITCH

* Consider the base-biased transistor in CE configuration as shown in Fig. (a).



(a)



(b)

Applying Kirchhoff's voltage rule to the input and output sides of this circuit, we get

$$V_{BB} = I_B R_B + V_{BE} \quad .... (1)$$

$$\text{and } V_{CE} = V_{CC} - I_C R_C \quad .... (2)$$

We shall treat V_{BB} as the dc input voltage V_i and V_{CE} as the dc output voltage V_o.

So, we have $V_i = I_B R_B + V_{BE}$ and $V_o = V_{CC} - I_C R_C$.

* In the case of Si transistor, as long as input V_i is less than 0.6 V, the transistor will be in cut off state and current I_C will be zero. Hence $V_o = V_{CC}$.
* When V_i becomes greater than 0.6 V the transistor is in active state with some current I_C in the output path and the output V_o decrease as the term $I_C R_C$ increases.
* With increase of V_i, I_C increases almost linearly and so V_o decreases linearly till its value becomes less than about 1.0V.
* Beyond this, the change becomes non linear and transistor goes into saturation state.
* With further increase in V_i the output voltage is found to decrease further towards zero though it may never become zero. If we plot the V_o vs V_i curve, [also called the transfer characteristics of the base-biased transistor (Fig. (b)], we see that between cut off state and active state and also between active state and saturation state there are regions of non-linearity showing that the transition from cutoff state to active state and from active state to saturation state are not sharply defined.

Working : As long as V_i is low and unable to forward-bias the transistor, V_o is high (at V_{CC}). If V_i is high enough to drive the transistor into saturation, then V_o is low, very near to zero. When the transistor is not conducting it is said to be switched off and when it is driven into saturation it is said to be switched on. This shows that if we define low and high states as below and above certain voltage levels corresponding to cutoff and saturation of the transistor, then we can say that a low input switches the transistor off and a high input switches it on. Alternatively, we can say that a low input to the transistor gives a high output and a high input gives a low output. The switching circuits are designed in such a way that the transistor does not remain in active state.

TRANSISTOR AS AN AMPLIFIER

* The process of increasing the amplitude of input signal without distorting its wave shape and without changing its frequency is known as amplification.
* A device which increases the amplitude of the input signal is called amplifier.

Common emitter amplifier

* For using the transistor as an amplifier we will use the active region of the V_o versus V_i curve.
* Input voltage of the CE amplifier increases its output voltage decreases and the output is said to be out of phase with the input.

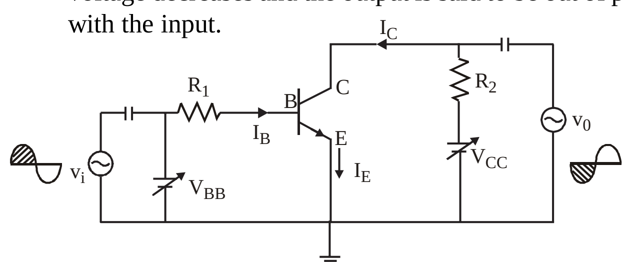


Figure : A simple circuit of a CE-transistor amplifier.

* **DC current gain :** It is the ratio of the collector current to the base current. dc current gain, $\beta = \frac{I_C}{I_B}$
* **AC current gain :** It is the ratio of the change in collector current to the change in base current at constant collector voltage. $\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$

* **AC voltage gain.** It is the ratio of the change in output voltage to the change in input voltage. It is denoted by A_V.

  or $A_V = \beta_{ac} \times$ resistance gain $= \beta_{ac} \times \frac{R_2}{R_1}$

* Trans or mutual conductance (g_m) : $\frac{\Delta I_C}{\Delta V_i} = \frac{\beta}{R_{in}}$.

  Its unit is $(ohm)^{-1}$ or mho or siemen.

* AC power gain $= \frac{\text{Change in output power}}{\text{Change in input power}}$

  $= \beta^2_{ac} \times$ resistance gain $= \beta^2_{ac} \times \frac{R_2}{R_1}$

Common base amplifier :

* In common base transistor amplifier the output signal is in phase with the input signal.
* **DC current gain :** The ratio of the collector current (I_C) to the emitter current (I_E). $\alpha = \frac{I_C}{I_E}$

  Since $I_C < I_E$, dc current gain is always less than 1. Its value lies between 0.95 to 0.999.
* **AC current gain :** It is the ratio of change in collector current to the change in emitter current at constant collector voltage.

  $\therefore \quad \alpha_{ac} = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_{CB}}$

* **AC voltage gain :** It is the ratio of change in output voltage to the change in input voltage.
  It is denoted by A_V.
  If ΔV_C is change in output voltage and ΔV_E is change in input voltage, then $A_V = \frac{\Delta V_C}{\Delta V_E}$

  $A_V = \alpha_{ac} \times$ resistance gain.
* **AC power gain :** It is the ratio of change in output power to the change in input power.

  AC power gain $= \frac{\text{Change in output power}}{\text{Change in input power}}$

  $= \alpha^2_{ac} \times$ resistance gain

NOTE

* Since $\beta_{ac} > \alpha_{ac}$, AC voltage gain in common emitter amplifier is very large as compared to that in common-base amplifier.

Relation between ~ and

For both types of amplifier,

$I_E = I_B + I_C$ or $\Delta I_E = \Delta I_B + \Delta I_C$

Dividing both sides of above equation by

ΔI_C, we get $\frac{\Delta I_E}{\Delta I_C} = \frac{\Delta I_B}{\Delta I_C} + 1$; but $\alpha = \frac{\Delta I_C}{\Delta I_E}$ and $\beta = \frac{\Delta I_C}{\Delta I_B}$,

$\therefore \quad \frac{1}{\alpha} = \frac{1}{\beta} + 1$ or $\beta = \frac{\alpha}{1-\alpha}$ or $\alpha = \frac{\beta}{\beta+1}$

If $\alpha = 0.99 \Rightarrow \beta = 99$

Example 9 :

In a transistor, the value of β is 50. Calculate the value of α.

Sol. $\beta = 50,\ \beta = \frac{\alpha}{1-\alpha} \Rightarrow 50 = \frac{\alpha}{1-\alpha} \Rightarrow 50 - 50\alpha = \alpha$

$\Rightarrow \alpha = \frac{50}{51} = 0.9850$

Example 10 :

Calculate the emitter current for which $I_b = 20\mu A$, $\beta = 100$

Sol. $\beta = 100,\ I_b = 20\ \mu A$

$I_c = \beta\, I_b = 100 \times 20 \times 10^{-6} = 2000\ \mu A$

$I_e = I_b + I_c = 20 + 2000 = 2020\ \mu A = 2.02 \times 10^{-3}\ A = 2.02\ mA$

Example 11 :

For a common emitter amplifier, current gain = 50. If the emitter current is 6.6 mA, calculate the collector and base current. Also calculate current gain, When emitter is working as common base amplifier.

Sol. $\beta = 50 : I_e = 6.6\ mA$

$\because \beta = \frac{I_c}{I_b} \quad \therefore I_c = \beta\, I_b = 50 I_b$ .... (i)

$I_e = I_c + I_b$ using equation (i) we get

$6.6 = 50\, I_b + I_b = 51\, I_b$ or $I_b = \frac{6.6}{51} = 0.129\ mA$

Hence $I_c = 50 \times \frac{6.6}{51} = 6.47\ mA$ and $\alpha = \frac{\beta}{1+\beta} = \frac{50}{51} = 0.98$

Example 12 :

Transistor with $\beta = 75$ is connected to common-base configuration. What will be the maximum collector current for an emitter current of 5 mA ?

Sol. $\beta = 75,\ I_e = 5\ mA$

$\beta = \frac{\alpha}{1-\alpha} \Rightarrow 75 = \frac{\alpha}{1-\alpha} \Rightarrow 75 - 75\alpha = \alpha$

$76\alpha = 75$ or $\alpha = \frac{75}{76}$; $\alpha = \frac{I_c}{I_e}$ $\therefore I_c = \alpha I_e = \frac{75}{76} \times 5 = 4.93\ mA$

FEEDBACK

Feedback are two types :

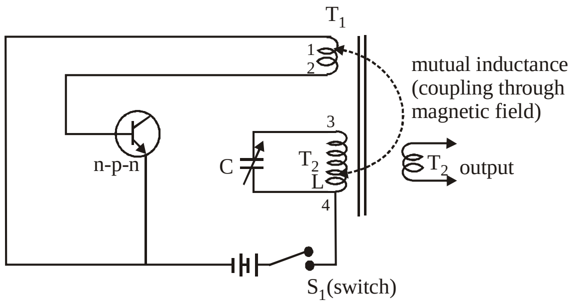
Positive feedback : When input and output are in the same phase then positive feedback is there. It is used in oscillators.

Negative feedback : If input and output are out of phase and some part of that is feedback to input is known as negative feedback. It is used to get constant gain amplifier.

TRANSISTOR AS AN OSCILLATOR

* In an oscillator, we get ac output without any external input signal.
* The output in an oscillator is self-sustained.

* A portion of the output power is returned back (feedback) to the input in phase with the starting power (positive feedback).



* The feedback can be achieved by inductive coupling (through mutual inductance) or LC or RC networks.
* The transistor is driven to saturation, then to cut-off, and then back to saturation. The time for change from saturation to cut-off and back is determined by the constants of the tank circuit or tuned circuit (inductance L of coil T_2 and C connected in parallel to it).
* The resonance frequency (f) of this tuned circuit determines the frequency at which the oscillator will oscillate.

$$f = \frac{1}{2\pi\sqrt{LC}}$$

* If the tank or tuned circuit is connected in the collector side, it is known as tuned collector oscillator.
* Gain of the complete amplifier with positive feedback.

$$A_{fb} = \frac{V_o}{V_i}$$

* If A is the gain of transistor CE amplifier (without feedback)

then $A = \frac{V_o}{V_i + mV_o}$, where m is feedback fraction.

This gives $A_{fb} = \frac{V_o}{V_i} = \frac{A}{1-mA}$.

* In order to produce continuous undamped oscillations at the output terminals of the amplifier, the positive feedback should be such that m . A = 1.

TRY IT YOURSELF - 1

Q.1 To obtain a P-type germanium semiconductor, it must be doped with –
(A) Arsenic (B) Antimony
(C) Indium (D) Phosphorus

Q.2 Which impurity is doped in Si to form N-type semiconductor
(A) Al (B) B
(C) As (D) None of these

Q.3 Function of rectifier is –
(A) To convert ac into dc (B) To convert dc into ac
(C) Both (A) and (B) (D) None of these

Q.4 The potential barrier, in the depletion layer, is due to –
(A) ions (B) holes
(C) electrons (D) forbidden band

Q.5 In a n-p-n transistor –
(A) holes moves from emitter to base
(B) holes move from base to collector
(C) negative charge moves from emitter to base
(D) negative charge moves from collector to base

Q.6 The value of β for a transistor, for which $\alpha = 0.95$, will be
(A) 19 (B) 91
(C) 1.9 (D) 0.19

Q.7 For a transistor, if $I_c/I_e = 0.96$, then current gain for common emitter is –
(A) 6 (B) 12
(C) 24 (D) 48

Q.8 A transistor is used in the common emitter mode as an amplifier. Then –
(a) The base-emitter junction is forward biased
(b) The base-emitter junction is reverse biased
(c) The input signal is connected in series with the voltage applied to bias the base emitter junction
(d) The input signal is connected in series with the voltage applied to bias the base collector junction
Correct options are –
(A) ab (B) bc
(C) cd (D) ac

Q.9 For a CE transistor amplifier, the audio signal voltage across the collector resistance of 2.0 kΩ is 2.0 V. Suppose the current amplification factor of the transistor is 100, What should be the value of R_B in series with V_{BB} supply of 2.0V if the dc base current has to be 10 times the signal current.
(A) 14 kΩ (B) 18 kΩ
(C) 10 kΩ (D) 5 kΩ

Q.10 In the above question, calculate the dc drop across the collector resistance.
(A) 20mA (B) 10mA
(C) 30mA (D) 50mA

ANSWERS

(1) (C)	**(2)** (C)	**(3)** (A)
(4) (A)	**(5)** (C)	**(6)** (A)
(7) (C)	**(8)** (D)	**(9)** (A)
(10) (B)		

LOGIC GATES

INTRODUCTION

* A logic gate is a digital circuit which is based on certain logical relationship between the input and the output voltages of the circuit.
* The logic gates are built using the semiconductor diodes and transistors.
* Each logic gate is represented by its characteristic symbol.
* The operation of a logic gate is indicated in a table, known as truth table. This table contains all possible combinations of inputs and the corresponding outputs.
* A logic gate is also represented by a Boolean algebraic expression. Boolean algebra is a method of writing logical equations showing how an output depends upon the combination of inputs. Boolean algebra was invented by George Boole.

LAWS OF BOOLEAN ALGEBRA

Basic OR, AND, and NOT operations are given :

OR	AND	NOT
$A + 0 = A$	$A . 0 = 0$	$A + \bar{A} = 1$
$A + 1 = 1$	$A . 1 = A$	$A . \bar{A} = 0$
$A + A = A$	$A . A = A$	$\bar{\bar{A}} . A = A$

Boolean algebra obeys commutative, associative and distributive law as given below :

Commutative laws :

$A + B = B + A$

$A . B = B . A$

Associative laws :

$A + (B + C) = (A + B) + C$

$A . (B . C) = (A . B) . C$

Distributive laws :

$A . (B + C) = A.B + A.C$

Some other useful identities :

(i) $A + AB = A$ (ii) $A . (A + B) = A$

(iii) $A + (\bar{A}B) = A + B$ (iv) $A . (\bar{A} + B) = A . B$

(v) $A + (B . C) = (A + B) . (A + C)$

(vi) $(\bar{A} + B).(A + C) = \bar{A}.C + B.A + B.C$

De Morgan's theorem :

First theorem : $\overline{A + B} = \bar{A}.\bar{B}$

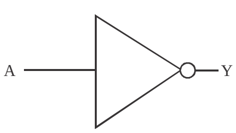
Second theorem : $\overline{A.B} = \bar{A} + \bar{B}$

BASIC LOGIC GATES

There are three basic logic gates. They are

(1) OR gate
(2) AND gate
(3) NOT gate.

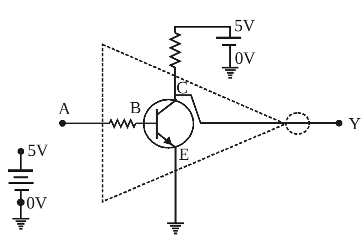
(a) NOT gate : **Truth table**



Input	Output
A	Y
0	1
1	0

Boolean algebra : $Y = \bar{A}$

The NOT gate, also called invertor, is obtained by employing npn transistor. The base (B) of the transistor is connected to A through a resistor R_b, while the emitter (E) is earthed. The collector is earthed through a resistor R_c & a 5 V battery.

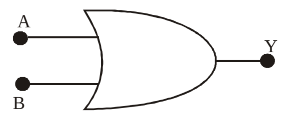


The operation of NOT gate can be understood in following steps:

(i) **A = 0.** The base of the transistor also gets earthed. Therefore, base emitter junction is not forward biased. Since base current is zero, the collector current is also zero. The transistor is said to be in cutoff mode. The output Y will be equal to the voltage of battery connected to collector i.e. 1.

(ii) **A = 1.** The base emitter junction gets forward biased and it leads to a large collector current. The transistor is said to have gone to saturation. The voltage drop across the resistor R_c is just equal to 5 V and the output Y is very nearly 0.

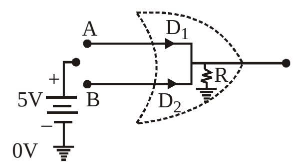
(b) OR gate : **Truth table**



Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Boolean algebra : $Y = A + B$

In practice, an OR gate can be realised by the electronic circuits making use of two ideal forward-biased junction diodes D_1 and D_2 as shown in figure.



The input voltage that can be applied at A or B is either 0 or 5 V. There are following possible cases:

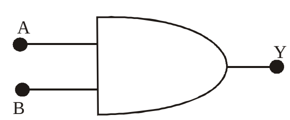
(i) **A = 0 and B = 0.** When both A and B are connected to each (0V) none of the diodes conduct and hence no voltage develops across resistor and accordingly output Y is 0.

(ii) **A = 0 and B = 1.** When A is connected to earth (0V) and B is connected to positive terminal of battery (5 V), junction diode D_1 does not conduct while diode D_2 conducts due to forward bias. If diode is an ideal one, output Ywill also be 5V or 1. (because potential drop across ideal diode D_2 is zero).

(iii) **A = 1 and B = 0.** In this case. reverse of above will happen i.e., diode D_1 will conduct due to forward bias and D_2 will not conduct. Thus, output will be 5V or 1. (D_1 is ideal)

(iv) **A = 1 and B = 1.** When A and B are connected to positive terminals of the battery (5V) both the diodes conduct, because both the outputs of the two diodes obtained across R are parallel, the net output Y = 5V or 1.

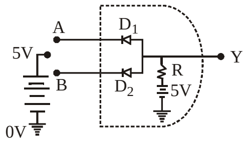
(c) AND gate :



Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Boolean algebra : $Y = A . B$

The AND gate can be realised by the electronic circuit making use of two ideal reverse-biased junction diodes D_1 and D_2 as shown in figure. The resistor R is connected to positive terminal of a 5V battery.



The operation of AND gate :

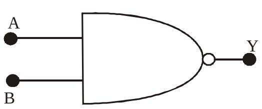
(i) **A = 0 and B = 0.** Both the diodes D_1 and D_2 get forward biased and hence conduct. The output Y will be the voltage drop across D_1 or D_2. Since diodes are ideal, no voltage drop can occur. Hence, the output Y is 0.

(ii) **A = 0 and B = 1.** The diode D_1 will conduct, but D_2 will remain ideal.
Now output Y is voltage across D_1 and hence is 0.

(iii) **A = 1 and B = 0.** The diode D_2 will conduct and diode D_1 will remain ideal. Now output Y is voltage across D_2 and hence is 0.

(iv) **A = 1 and B = 1.** Both the diodes will not conduct. The output Y will be equal to battery voltage 5V and hence is 1.

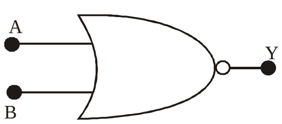
(d) **NAND gate :**
Output of AND gate is connected to the input of NOT gate.



Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Boolean algebra : $Y = \overline{A \cdot B}$

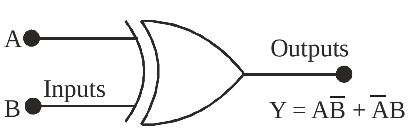
(e) **NOR gate :**
Output of OR gate is connected to the input of NOT gate.



Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Boolean algebra : $Y = \overline{A + B}$

(f) **Exclusive OR gate (XOR gate) :**
Output of XOR is 1 only when inputs are complement to each other.



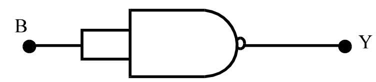
Truth table of XOR gate

A	B	$Y = A\overline{B} + \overline{A}B$
0	0	0
0	1	1
1	0	1
1	1	0

Note : The NAND or NOR gate is the universal building block of all digital circuits. Repeated use of NAND gates (or NOR gates) gives other gates. Therefore, any digital system can be achieved entirely from NAND or NOR gates.

* **NOT gate from NAND :**

(a) Figure

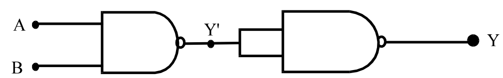


(b) Truth table

A	B	$Y = \overline{A.B}$
0	0	1
1	1	0

* **AND gate from NAND :**

(a) Figure

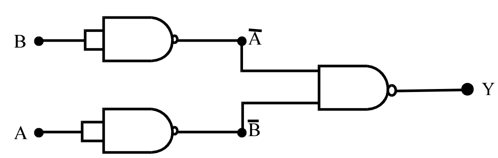


(b) Truth table

A	B	$\overline{A.B} = Y^1$	$Y = \overline{Y}^1$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

* **OR gate from NAND :**

(a) Figure

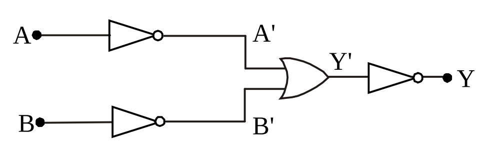


(b) Truth table

A	B	$\overline{A}$	$\overline{B}$	$Y = (\overline{A.B})$
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

Example 13 :

In the circuit shown in the figure, identify the equivalent gate of the circuit and make its truth table



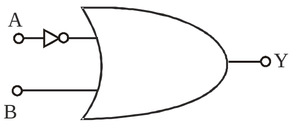
Sol. AND GATE

Truth table

Input		Output
A	B	Y
1	0	0
0	1	0
0	0	0
1	1	1

TRY IT YOURSELF - 2

Q.1 The Boolean equation for the circuit given in figure -is –



(A) $Y = A + \overline{B}$ (B) $Y = \overline{A + B}$

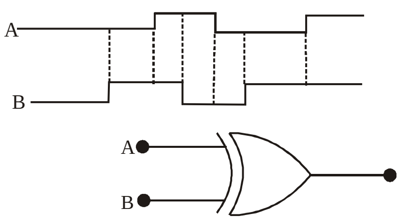
(C) $Y = \overline{A} + B$ (D) $Y = \overline{A} + \overline{B}$

Q.2 According to the laws of Boolean algebra, the expression $(A + AB)$ is equal to

(A) A (B) AB

(C) B (D) $\overline{A}$

Q.3 Determine the output wave form for the circuit given below, if the input waveforms are as indicated by A and B.



Q.4 Mark the correct statement –

(A) both XOR and NAND gates can be used as universal gates

(B) both NAND and NOR gates can be used as universal gates

(C) both NOR and XOR gates can be used as universal gates

(D) only NAND gates can be used as universal gate but NOR gate cannot be used as universal gate.

Q.5 If A= B = 1 then in terms of Boolean algebra $A + \overline{B}$ equals

(A) $\overline{A}$ (B) $\overline{B}$

(C) A or B (D) $\overline{A + B}$

Q.6 In the Boolean algebra Y = A.B indicates that –

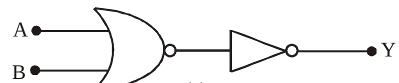
(A) output Y exists when either input A or input B exists

(B) output Y exists only both inputs A and B exist

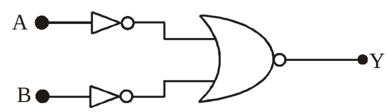
(C) output Y exists when either input A exists or input B exists but not when both inputs A and B exist

(D) product of A and B is Y

Q.7 You are given the two circuits as shown in figure. Show that circuit (a) acts as OR gate while the circuit (b) acts as AND gate.



(a)



(b)

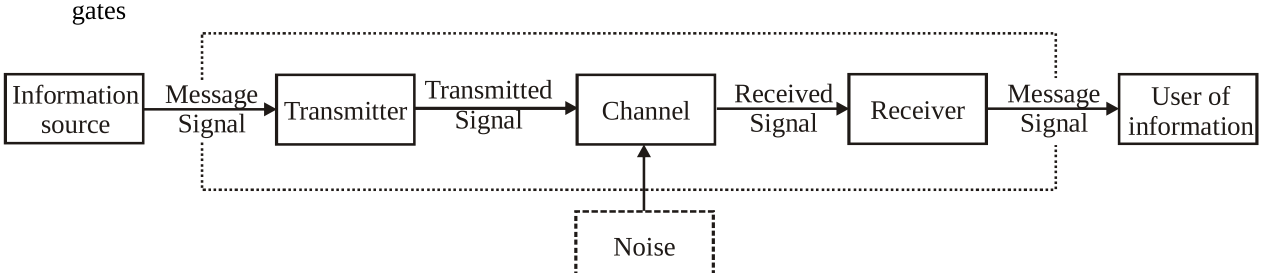
PRINCIPLES OF COMMUNICATION SYSTEMS

INTRODUCTION

Communication means transmission of information. Everyone experiences the need to impart or receive information continuously in the surrounding and for this, we speak, listen, send message by a messenger, use coded signalling methods through smoke or flags or beating of drum etc. and these days we are using telephones, TV, radio, satellite communication etc. The aim of this section is to introduce the concepts of communicative namely the mode of communication, the need for modulation, production and detection of amplitude modulation.

Elements of a Communication System :

Every communication system has three essential elements (i) transmitter (ii) medium/channel (iii) receiver



Transmitter converts the message signal into an electric signal and transmits through channel. The receiver receives the transmitted signal and reconstructs the original message signal to the end user. There are two basic modes of communication: (i) point-to-point and (ii) broadcast.

In point-to-point communication mode, communication takes place over a link between a single transmitter and a receiver as in telephony. In the broadcast mode, there are a large number of receivers corresponding to a single transmitter. Radio and television are most common examples of broadcast mode of communication. However the communication system can be classified as follows :

Types of Communication Systems

On the basis of nature of Information
(1) Speech Transmission (Radio)
(2) Picture Transmission (TV)
(3) Facsimile Transmission (Fax)
(4) Data Transmission Intermet

On the basis of signal transmitted
(1) Analog
(2) Digital

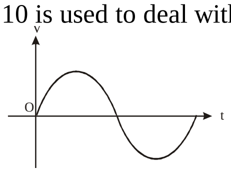
On the basis of transmission Channel
(1) Line communication
(a) Two wire Transmission line
(b) Coaxial cable
(c) Optical fibre
(2) Space communication

On the basis of type of modulation
(1) Continuous wave modulation
(a) Amplitude (AM)
(b) Frequency (FM)
(c) phase (PM)
(2) Pulse Modulation
(a) PAM
(b) PTM – PPM, PWM
(c) PCM

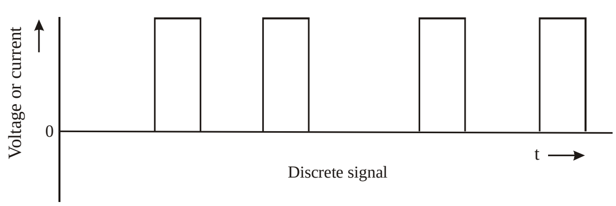
BASIC TERMINOLOGY USED IN ELECTRONIC COMMUNICATION SYSTEMS

(i) Transducer : Transducer is the device that converts one form of energy into another. Microphone, photo detectors and piezoelectric sensors are types of transducer. They convert information into electrical signal.

(ii) Signal : Signal is the information converted in electrical form. Signals can be analog or digital. Sound and picture signals in TV are analog.
It is defined as a single-valued function of time which has a unique value at every instant of time.
Analog Signal : A continuously varying signal (Voltage or Current) is called an analog signal. A decimal number with system base 10 is used to deal with analog signal.



Digital Signal : A signal that can have only discrete stepwise values is called a digital signal. A binary number system with base 2 is used to deal with digital signals.



(iii) Noise : There are unwanted signals that tend to disturb the transmission and processing of message signals. The source of noise can be inside or outside the system.

(iv) Transmitter: A transmitter processes the incoming message signal to make it suitable for transmission through a channel and subsequent reception.

(v) Receiver: A receiver extracts the desired message signals from the received signals at the channel output.

(vi) Attenuation: It is the loss of strength of a signals while propagating through a medium. It is like damping of oscillations.

(vii) Amplification : It is the process of increasing the amplitude (and therefore the strength) of a signal using an electronic circuit called the amplifier. Amplification is absolutely necessary to compensate for the attenuation of the signal in communication systems.

(viii) Range : It is the largest distance between the source and the destination upto which the signal gets received with sufficient strength.

(ix) Bandwidth : It is the frequency range over which an equipment operates or the portion of the spectrum occupied by the signal.

(x) Modulation : The original low frequency message/ information signal cannot be transmitted to long distances. So, at the transmitter end, information contained in the low frequency message signal is superimposed on a high frequency wave, which acts as a carrier of the information. This process is known as modulation.

(xi) Demodulation : The process of retrieval of original information from the carrier wave at the receiver end is termed as demodulation. This process is the reverse of modulation.

(xii) Repeater : A repeater acts as a receiver and a transmitter. A repeater picks up the signal which is coming from the transmitter, amplifies and retransmits it with a change in carrier frequency. Repeaters are necessary to extend the range of a communication system. A communication satellite is basically a repeater station in space.

BANDWIDTH

Bandwidth of signals : The difference of maximum and minimum frequency in the range of each signal is called bandwidth of that signal.

Service	Frequency bands	Comments
Standard AM broadcast	540-1600 kHz	
FM broadcast	88-108 MHz	
Television	54-72 MHz 76-88 MHz 174-216 MHz 420-890 MHz	VHF (very high frequencies) TV UHF (ultra high frequencies) TV
Cellular Mobile Radio	896-901 MHz 840-935 MHz	Mobile to base station Base station to mobile
Satellite Communication	5.925-6.425 GHz 3.7-4.2 GHz	Uplink Downlink

PROPAGATION OF ELECTROMAGNETIC WAVES

In case of radio waves communication, an antenna at the transmitter radiates the electromagnetic waves (em waves). The em waves travel through the space and reach the receiving antenna at the other end. As the em wave travels away from the transmitter, their strength keeps on decreasing. Many factors influence the propagation of em waves including the path they follow. The composition of the earth's atmosphere also plays a vital role in the propagation of em waves, as summarised below.

Layers of atmosphere and their Interaction with the propagating em waves

Atmospheric stratum (layer)	Height over earth's surface (approx)	Exists during	Frequencies most likely affected
1. Troposphere	10 km	Day and night	VHF (upto several GHz)
2. Ionosphere			
(i) D (part of stratosphere)	65-75 km	Day only	Reflects LF, absorbs MF & HF to some degree
(ii) E (part of stratosphere)	100 km	Day only	Helps surface waves, reflects HF
(iii) F_1 (Part of Mesosphere)	170-190km	Daytime, merges with F_2 at night	Partially absorbs HF waves yet allowing them to reach F_2
(iv) F_2 (Thermosphere)	300 km at night, 250-400 km during daytime	Day and night	Efficiently reflects HF waves particularly at night

GROUND WAVE PROPAGATION

(a) The radio waves which travel through atmosphere following the surface of earth are known as ground waves or surface waves and their propagation is called ground wave propagation or surface wave propagation.

(b) The ground wave transmission becomes weaker with increase in frequency because more absorption of ground waves takes place at higher frequency during propagation through atmosphere.

(c) The ground wave propagation is suitable for low and medium frequency i.e. upto 20 MHz only.

(d) The ground wave propagation is generally used for local band broadcasting and is commonly called medium wave.

(e) The maximum range of ground or surface wave propagation depends on two factors :
(i) The frequency of the radio waves and
(ii) Power of the transmitter

SKY WAVE PROPAGATION

(a) The sky waves are the radio waves of frequency between 2MHz to 30 MHz.

(b) The ionoopheric layer acts as a reflector for a certain range of frequencies (3 to 30 MHz). Electromagnetic waves of frequencies higher than 30 MHz penetrate the ionosphere and escape.

(c) The highest frequency of radiowaves which when sent straight (i.e. normally) towards the layer of ionosphere gets reflected from ionosphere and returns to the earth is called critical frequency. . If is given by $f_c = 9\,(N_{max})^{1/2}$, where N is the number density of electron/m^3.

SPACE WAVE PROPAGATION

(a) The space waves are the radiowaves of very high frequency (i.e. between 30 MHz. to 300 MHz or more).

(b) The space waves can travel through atmosphere from transmitter antenna to receiver antenna either directly or after reflection from ground in the earth's troposphere region. That is why the space wave propagation is also called as tropospherical propagation or line of sight propagation.

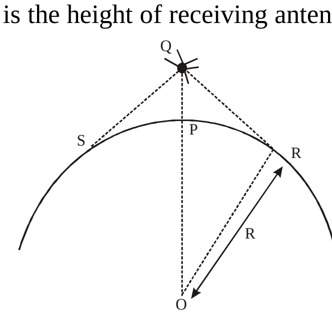
(c) The range of communication of space wave propagation can be increased by increasing the heights of transmitting and receiving antenna.

(d) If the transmitting antenna is at a height h_T, then you can show that the distance to the horizontal d_T is given as

$d_T = = \sqrt{2Rh_T}$, where R is the radius of the earth (approximately 6400 km). d_T is also called the radio maximum line-of sight distance d_m between the two antennas having heights h_T and h_R above the earth is given by :

$$d_M = \sqrt{2Rh_T} + \sqrt{2Rh_R}$$

where h_R is the height of receiving antenna.



MODULATION

It is a process by which any electrical signal called input, baseband or modulating signal, is mounted onto another signal of high frequency which is known as carrier signal. It is defined as the process by which some characteristic (called parameter) of carrier signal is varied in accordance with the instantaneous value of the baseband signal.

The signal which results from this process is known as modulated signal.

Need for Modulation :

(i) To avoid interference: If many modulating signals travel directly through the same transmission channel, they will interfere with each other and result in distortion.

(ii) To design antennas of practicable size: The minimum height of antenna (not of antenna tower) should be $\lambda/4$ where λ is wavelength of modulating signal. This minimum size becomes impracticable because the frequency of the modulating signal can be upto 5 kHz which corresponds to a wavelength of $3 \times 10^8/5 \times 10^{-3} = 60$ km. This will require an antenna of the minimum height of $\lambda/4 = 15$ km. This size of an antenna is not practical.

(iii) Effective Power Radiated by an Antenna : A theoretical study of radiation from a linear antenna (length ℓ) shows that the power radiated is proportional to (frequency)^2 i.e.$(\ell/\lambda)^2$. For a good transmission, we need high powers and hence this also points out to the need of using high frequency transmission.

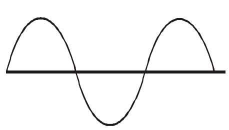
The above discussion suggests that there is a need for translating the original low frequency baseband message signal into high frequency wave before transmission. In doing so, we take the help of a high frequency signal, which we already know now, is known as the carrier wave, and a process known as modulation which attaches information to it. The carrier wave may be continuous (sinusoidal) or in the form of pulses.

CARRIER WAVE : SINUSOIDAL

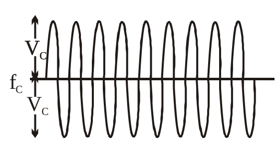
A sinusoidal carrier wave can be represented as

$$c(t) = A_C \sin(\omega_c t + \phi)$$

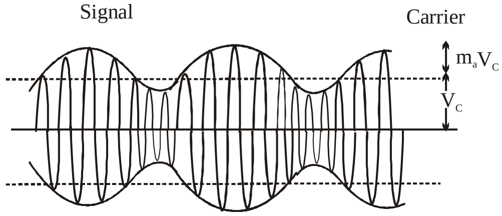
where c (t) is the signal strength (voltage or current), A_c is the amplitude, $\omega_c = (2\pi f_c)$ is the angular frequency and ϕ is the initial phase of the carrier wave. Thus, modulation can be affected by varying, any of three parameters, viz A_c, ω_c and ϕ of the carrier wave can as per the parameter of the message or information signal. This results in three types of modulation:(i) Amplitude modulation (AM), (ii) Frequency modulation (FM), (iii) Phase modulation (PM).



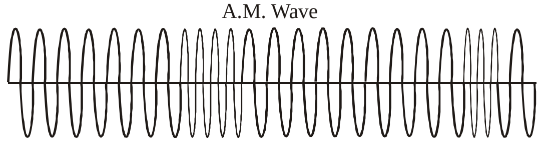
Signal



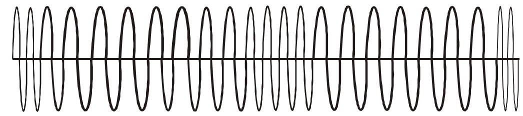
Carrier



A.M. Wave



Frequency modulated wave



Phase modulate wave

CARRIER WAVE PULSES

Similarly, the significant characteristics of a pulse are: Pulse Amplitude, Pulse duration or pulse Width, and pulse Position (denoting the time of rise or fall of the pulse amplitude) Hence, different types of pulse modulation are (a) pulse amplitude modulation (PAM), (b) Pulse duration modulation (PDM) or pulse width modulation (PWM), and (c) Pulse position modulation (PPM).

AMPLITUDE MODULATION

In amplitude modulation the amplitude of the carrier is varied in accordance with the information signals.

Let $c(t) = A_c \sin \omega_c t$ represent carrier wave and

$m(t) = A_m \sin \omega_m t$ resent the message or the modulating signal where $\omega_m = 2\pi f_m$ is the angular frequency of the message signal. The modulated signal $c_m(t)$ can be written as $c_m(t) = (A_c + A_m \sin \omega_m t) \sin \omega_c t$

$$= A_c\left(1+\frac{A_m}{A_c}\sin\omega_m t\right)\sin\omega_c t \quad \text{..........(1)}$$

Note that the modulated signal now contains the message signal & it can be written as :

$$c_m(t) = A_c \sin\omega_c t + \mu A_c \sin\omega_m t \sin\omega_c t \quad \text{........... (2)}$$

Here $\mu = A_m/A_c$ is the modulation index

In practice, μ is kept ≤ 1 to avoid distortion.

Using the trigonometric relation

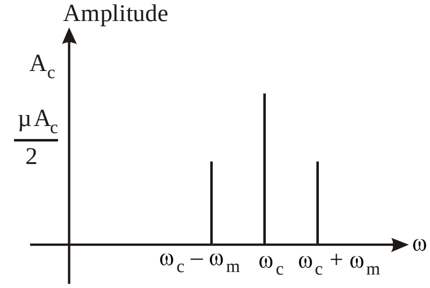
$$\sin A \sin B = 1/2 (\cos(A-B) - \cos(A+B)),$$

we can write $c_m(t)$ of eq. as

$$c_m = A_c \sin\omega_c t + \frac{\mu A_c}{2}\cos(\omega_c - \omega_m)t$$

$$-\frac{\mu A_c}{2}\cos(\omega_c + \omega_m)t \quad \text{..........(3)}$$

Here $\omega_c - \omega_m$ and $\omega_c + \omega_m$ are respectively called the called the lower side and upper side frequencies. The modulated signal now consists of the carrier wave of frequency ω_c plus two sinusoidal waves each with a frequency slightly different from, know as side bands. The frequency spectrum of the amplitude modulated signal is shown in figure :



As long as the broadcast frequencies (carrier waves) are sufficiently spaced out so that sidebands do not overlap, different stations can operate without interfering with each other.

Example 14 :

A message signal of frequency 10 kHz and peak voltage of 10 volts is used to modulate a carrier of frequency 1 Mhz and peak voltage of 20 volts. Determine (a) modulation index,
(b) the side bands produced.

Sol. (a) Modulation index = 10/20 = 0.5
(b) The side bands are at (1000 + 10 kHz) = 1010 kHz
and (1000 – 10 kHz) = 990 kHz.

Disadvantages of AM

1. **Low frequency :** Power carried by side band frequencies is only 1/3 of total power even when 100% modulation.
If modulation is 50%, this becomes 1/9.
2. **Small operating range :** Due to small useful power, the message cannot be transmitted over a long distance.
3. **Noisy reception :** The reception becomes noisy due to reproduction of atmospheric and other electrical disturbance.

FREQUENCY MODULATION (FM)

* Frequency modulation is defined as the system in which the frequency of carrier wave is varied in accordance with the instantaneous value of the modulating voltage
* The amplitude of FM carrier is constant, so the transmitted power is constant. Hence, it becomes more efficient in comparison to AM.
* Frequency spectrum allocated for FM (88 MHz to 108 MHz) is much more than AM (512 kHz to 1710 kHz). Hence noise is much less.
* In FM carrier wave, band width is much larger than AM wave.

TRY IT YOURSELF - 3

Q.1 Modulation as well as band width increases in case of–
(A) AM (B) FM
(C) VSB (D) DSB

Q.2 Which of the following frequencies will be suitable for receiver beyond-the horizon communication using sky waves?
(A) 10 kHz (B) 10 MHz
(C) 1 GHz (D) 1000 GHz

Q.3 The band width of optical fibre communication is –
(A) 10^6 to 10^9 Hz (B) 10^{13} to 10^{15} Hz
(C) 10^9 to 10^{11} Hz (D) None of these

Q.4 Calculate the length of half wave dipole antenna at 200MHz.
(A) 0.75 (B) 2.30
(C) 1.20 (D) 5.10

Q.5 To cover a population of 20 lakh, a transmission tower should have a height: (radius of the earth = 6400 km, population per square km = 1000)
(A) 25 m (B) 50 m
(C) 75 m (D) 100 m

Q.6 In AM wave the modulation index is 100%. If the carrier is suppressed the percentage saving in power will be –
(A) 66.6% (B) 50%
(C) 75% (D) None of these

Q.7 An audio signal 20 sin 2π (1500t) amplitude modulates 80 sin 2π (10^6t). The band width required to transmit the AM wave is –
(A) 3 KHz (B) 2.5 KHz
(C) 2 KHz (D) 2.8 KHz

Q.8 In a FM system, a 7 kHz signal modulates 107.6 MHz so that the frequency deviation is 50 kHz. The carrier swing will be–
(A) 7.143 (B) 8
(C) 10 (D) None of these

ANSWERS

(1) (B)	**(2)** (B)	**(3)** (B)
(4) (A)	**(5)** (B)	**(6)** (A)
(7) (A)	**(8)** (A)	

ADDITIONAL EXAMPLES

Example 1 :

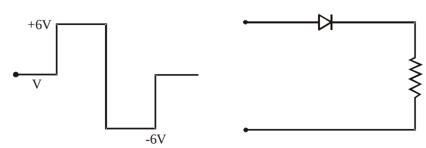
Pure Si at 300 K has equal electron (n_e) and hole (n_h) con- . . . . 1.5×10^{16} m^{-3}. Doping by indium increases n_h to 3×10^{22} m^{-3}. Calculate n_e in the doped Si.

Sol. For a doped semi-conductor in thermal equilibrium
$n_e n_h = n_i^2$ (Law of mass action)

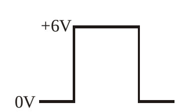
$$n_e = \frac{n_i^2}{n_h} = \frac{(1.5\times10^{16})^2}{3\times10^{22}} = 7.5 \times 10^9\ m^{-3}.$$

Example 2 :

What is an ideal diode ? Draw the output waveform across the load resistor R, if the input waveform as shown in the figure.



Sol. An ideal diode has zero resistance when forward biased and infinite resistance when it is reversed biased.
Output wave form is shown in fig.



Example 3 :

In an NPN transistor 10^{10} electrons enter the emitter in 10^{-6} s and 2% electrons recombine with holes in base, then current gain α and β are :

Sol. Emitter current $I_e = \frac{Ne}{t} = \frac{10^{10}\times1.6\times10^{-19}}{10^{-6}} = 1.6$ mA

Base current $I_b = \frac{2}{100} \times 1.6 = 0.032$ mA

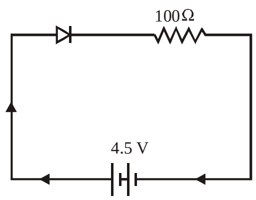
But, $I_e = I_c + I_b$

$\therefore \quad I_c = I_e - I_b = 1.6 - 0.032 = 1.568$ mA

$$\therefore \quad \alpha = \frac{I_c}{I_e} = \frac{1.568}{1.6} = 0.98 \text{ and } \beta = \frac{I_c}{I_b} = \frac{1.568}{0.032} = 49$$

Example 4 :

Figure shows a diode connected to an external resistance and an e.m.f. Assuming that the barrier potential developed in diode is 0.5 V obtain the value of current in the circuit in milliampere.



Sol. E = 4.5 V, R = 100 Ω

Voltage drop across p-n junction = 0.5 V

Effective voltage In the circuit V = 4.5 – 0.5 = 4.0 V

Current in the circuit

$$I = \frac{V}{R} = \frac{4.0}{100} = 0.04 \text{ A} = 0.04 \times 1000 \text{ mA} = 40 \text{ mA}$$

Example 5 :

The base current is 100 μA and collector current is 3 mA.

(a) Calculate the values of β, I_e and α.

(b) A change of 20 μA in the base current produces a change of 0.5 mA in the collector current. Calculate β_{ac}.

Sol. $I_b = 100\ \mu A = 0.100$ mA, $I_c = 3$mA

(a) $\beta = \frac{I_c}{I_b} = \frac{3}{0.100} = 30$

$$\alpha = \frac{\beta}{1+\beta} = \frac{30}{1+30} = \frac{30}{31} = 0.97$$

and $I_e = \frac{I_c}{\alpha} = \frac{3 \times 31}{30} = 3.1$ mA

(b) $\Delta I_b = 20\ \mu A = 0.02$ mA, $\Delta I_c = 0.5$ mA

$$\therefore \beta_{ac} = \frac{\Delta I_c}{\Delta I_b} = \frac{0.5}{0.02} = 25$$

QUESTION BANK

CHAPTER 8 : SEMICONDUCTOR & COMMUNICATION SYSTEMS

EXERCISE - 1 [LEVEL-1]

Choose one correct response for each question.

PART 1 : CLASSIFICATION OF METALS, CONDUCTORS & SEMICONDUCTORS

Q.1 At 0 K, silicon behave as –
(A) super conductor (B) conductor
(C) Insulator (D) none of these

Q.2 In semiconductors, at room temperature
(A) the valence band is partially empty and the conduction band is partially filled.
(B) the valence band is completely filled and the conduction band is partially filled.
(C) the valence band is completely filled.
(D) the conduction band is completely empty.

Q.3 Choose the correct statement-
(A) The energy band above the valence band is called the conduction band.
(B) The gap between the top of the valence band and bottom of the conduction band is called the energy band gap.
(C) The resistance of semiconductors is not as high as that of the insulators.
(D) All of these

PART 2 : INTRINSIC AND EXTRINSIC SEMICONDUCTOR

Q.4 Choose the correct statement –
(A) For n-type semiconductors, $n_e >> n_h$.
(B) For p-type semiconductors, $n_h >> n_e$.
(C) The electron and hole concentration in a semiconductor in thermal equilibrium is given by $n_e n_h = n_i^2$
(D) All of these

Q.5 An n-type and p-type silicon can be obtained by doping pure silicon with
(A) arsenic and phosphorous respectively
(B) indium and aluminum respectively
(C) phosphorous and indium respectively
(D) aluminium and boron respectively

Q.6 The probability of electrons to be found in the conduction band of an intrinsic semiconductor of finite temperature –
(A) increases exponentially with increasing band gap.
(B) decreases exponentially with increasing band gap.
(C) decreases with increasing temperature.
(D) is independent of the temperature and band gap.

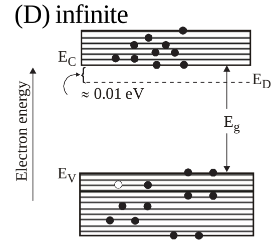
Q.7 In n-type semiconductor, majority charge carriers are
(A) holes (B) protons
(C) neutrons (D) electrons

Q.8 Hole is –
(A) an anti-particle of electron.
(B) a vacancy created when an electron leaves a covalent bond.
(C) absence of free electrons.
(D) an artifically created particle.

Q.9 If a small amount of antimony is added to germanium crystal
(A) its resistance is increased.
(B) it becomes a p-type semiconductor.
(C) there will be more free electrons than holes in the semiconductor.
(D) none of these

Q.10 In intrinsic semiconductor at room temperature, number of electrons and holes are
(A) equal (B) zero
(C) unequal (D) infinite

Q.11 Energy band diagram shown represents –



(A) n-type semiconductor
(B) p-type semiconductor
(C) intrinsic semiconductor
(D) None of these

PART 3 : P-N JUNCTION

Q.12 The electrical resistance of depletion layer is large because
(A) It has no charge carriers.
(B) It has a large number of charge carriers.
(C) It contains electrons as charge carriers.
(D) It has holes as charge carriers.

Q.13 During the formation of p-n junction –
(A) holes diffuse from p-side to n-side.
(B) electrons diffuse from n-side to p-side.
(C) holes diffuse from n-side to p-side.
(D) Both (A) and (B)

Q.14 The depletion layer in silicon diode is 1 μm wide and the knee potential is 0.6 V, then the electric field in the depletion layer will be
(A) Zero (B) $0.6\ Vm^{-1}$
(C) 6×10^4 V/m (D) 6×10^5 V/m

Q.15 Choose the correct statement for p-n junction–
(A) When an electron diffuses from n $\rightarrow$ p, it leaves behind an ionised donor on n-side.
(B) When a hole diffuses from p $\rightarrow$ n, it leaves behind an ionised acceptor (negative charge).
(C) When an electron diffuses from n $\rightarrow$ p, it leaves behind an ionised donor on p-side.
(D) Both (A) and (B)

Q.16 The dominant mechanisms for motion of charge carriers in forward and reverse biased silicon P-N junctions are
(A) Drift in forward bias, diffusion in reverse bias.
(B) Diffusion in forward bias, drift in reverse bias.
(C) Diffusion in both forward and reverse bias.
(D) Drift in both forward and reverse bias.

Q.17 During formation of a p-n junction, two important processes occurring are –
(A) drift and diffusion of charge carriers.
(B) diffusion and breakdown of atoms.
(C) bond formation and electron sharing among nuclei.
(D) hole & electron transfer from top to bottom.

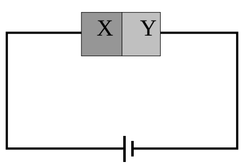
PART 4 : SEMICONDUCTOR DIODE

Q.18 On increasing the reverse bias to a large value in a PN-junction diode, current
(A) Increases slowly (B) Remains fixed
(C) Suddenly increases (D) Decreases slowly

Q.19 Zener breakdown in a semi-conductor diode occurs when
(A) Forward current exceeds certain value
(B) Reverse bias exceeds certain value
(C) Forward bias exceeds certain value
(D) Potential barrier is reduced to zero

Q.20 Barrier potential of a P-N junction diode does not depend on
(A) Temperature (B) Forward bias
(C) Doping density (D) Diode design

Q.21 A semiconductor X is made by doping a germanium crystal with arsenic (Z = 33). A second semiconductor Y is made by doping germanium with indium (Z = 49). The two are joined end to end and connected to a battery as shown. Which of the following statements is correct

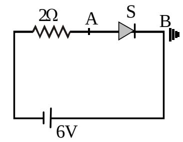


(A) X is P-type, Y is N-type and the junction is forward biased.
(B) X is N-type, Y is P-type and the junction is forward biased.
(C) X is P-type, Y is N-type and the junction is reverse biased.
(D) X is N-type, Y is P-type and the junction is reverse biased.

Q.22 In a semiconductor diode, the barrier potential offers opposition to –
(A) holes in P-region only
(B) free electrons in N-region only
(C) majority carriers in both regions
(D) majority as well as minority carriers in both regions.

Q.23 No bias is applied to a P-N junction, then the current
(A) Is zero because the number of charge carriers flowing on both sides is same.
(B) Is zero because the charge carriers do not move.
(C) Is non-zero.
(D) None of these.

Q.24 The diode shown in the circuit is a silicon diode. The potential difference between the points A and B will be



(A) 6 V (B) 0.6 V
(C) 0.7 V (D) 0 V

PART 5 : RECTIFIER

Q.25 The maximum efficiency of full wave rectifier is
(A) 100% (B) 25.20%
(C) 40.2% (D) 81.2%

Q.26 In a full wave rectifiers, input ac current has a frequency 'ν'. The output frequency of current is
(A) ν/2 (B) ν
(C) 2ν (D) None

Q.27 In half wave rectifier peak value of sinusoidal signal is 10V. Determine D.C. component at output –
(A) $\frac{10}{\sqrt{2}}$ V (B) $\frac{10}{\pi}$ V (C) 10 V (D) $\frac{20}{\pi}$ V

Q.28 In a half wave rectifier circuit operating from 50Hz mains frequency, the fundamental frequency in the ripple would be
(A) 25 Hz (B) 50 Hz
(C) 70.7 Hz (D) 100 Hz

PART 6 : SPECIAL PURPOSE PN JUNCTION DIODES

Q.29 Zener diode is used as
(A) Half wave rectifier (B) Full wave rectifier
(C) ac voltage stabilizer (D) dc voltage stabilizer

Q.30 A Zener diode is specified as having a breakdown voltage of 9.1 V, with a maximum power dissipation of 364 mW. What is the maximum current the diode can handle?
(A) 40 mA (B) 60 mA
(C) 50 mA (D) 45 mA

Q.31 Opto electronic devices are
(A) discharge tubes
(B) bulbs
(C) light based semiconductor diodes
(D) CFL

Q.32 GaAs is better than Si for solar cells due to –
(A) Its higher absorption coefficient.
(B) Its lower absorption coefficient.
(C) Its higher band gap
(D) Its lower band gap

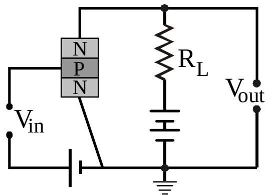
Q.33 An LED is used to
(A) convert light energy into electrical energy.
(B) convert light energy into heat energy.
(C) convert heat energy into light energy.
(D) convert electrical energy into light energy.

PART 7 : JUNCTION TRANSISTOR

Q.34 The emitter-base junction of a transistor is …… biased while the collector-base junction is ……. biased

(A) Reverse, forward (B) Reverse, reverse
(C) Forward, forward (D) Forward, reverse

Q.35 An NPN-transistor circuit is arranged as shown in figure. It is



(A) A common base amplifier circuit
(B) A common emitter amplifier circuit
(C) A common collector amplifier circuit
(D) Neither of the above

Q.36 The part of a transistor which is heavily doped to produce a large number of majority carriers, is

(A) Base (B) Emitter
(C) Collector (D) None of these

Q.37 In the study of transistor as an amplifier, if $\alpha = I_C/I_E$ and $\beta = I_C/I_B$, where I_C, I_B and I_E are the collector, base and emitter currents, then

(A) $\beta = \dfrac{1-\alpha}{\alpha}$ (B) $\beta = \dfrac{\alpha}{1-\alpha}$ (C) $\beta = \dfrac{\alpha}{1+\alpha}$ (D) $\beta = \dfrac{1+\alpha}{\alpha}$

Q.38 In a CE transistor configuration, the ratio of power gain to voltage gain is

(A) α (B) β / α
(C) $\beta\alpha$ (D) β

Q.39 Transistor working as an amplifier operates in its active region of characteristics only when –

(A) The emitter junction is forward biased and the collector junction is reverse biased.
(B) The emitter junction is reverse biased.
(C) The collector junction is forward biased.
(D) The emitter junction is reverse biased and the collector junction is forward biased

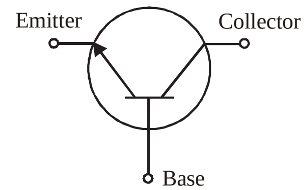
Q.40 A transistor has three impurity regions. All the three regions have different doping levels. In order of increasing doping level, the regions are

(A) emitter, base and collector
(B) collector, base and emitter
(C) base, emitter and collector
(D) base, collector, and emitter

Q.41 In case of N-P-N transistors the collector current is always less than the emitter current because –

(A) collector side is reverse biased and emitter side is forward biased.
(B) a few electrons are lost in the base and only the remaining ones reach the collector.
(C) collector side is forward biased and emitter side is reverse biased.
(D) collector being reverse biased attracts less electrons.

Q.42 Symbol shown represents –



(A) n-p-n transistor (B) p-n-p transistor
(C) n-p-p transistor (D) None of these

Q.43 For a transistor amplifier, the voltage gain

(A) remains constant for all frequencies.
(B) is high at high and low frequencies and constant in the middle frequency range.
(C) is low at high and low frequencies and constant at mid frequencies.
(D) none of these

Q.44 Reciprocal of slope of linear part of output characteristics (I-V) of a n-p-n CE transistor is equal to –

(A) 1 (B) 0
(C) r_0 (D) $1/r_0$

Q.45 In an n-p-n transistor in CE configuration, when V_{CE} is increased, then

(A) I_B increases & I_C increases proportionally
(B) I_B increases and I_C remains constant
(C) effect on I_B is negligible.
(D) both I_B and I_C remain nearly constant

Q.46 If β, R_L and r are the ac current gain, load resistance and the input resistance of a transistor respectively in CE configuration, the voltage and the power gains respectively are

(A) $\beta\dfrac{R_L}{r}$ & $\beta^2\dfrac{R_L}{r}$ (B) $\beta\dfrac{r}{R_L}$ & $\beta^2\dfrac{r}{R_L}$

(C) $\beta\dfrac{R_L}{r}$ & $\beta\left(\dfrac{R_L}{r}\right)^2$ (D) $\beta\dfrac{r}{R_L}$ & $\beta\left(\dfrac{r}{R_L}\right)^2$

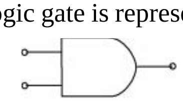
Q.47 Input resistance (r_i) of a transistor in CE configuration is –

(A) $\left[\dfrac{\Delta V_{BE}}{\Delta I_B}\right]_{V_{CE}}$ (B) $\left[\dfrac{\Delta V_{CE}}{\Delta I_B}\right]_{V_{BE}}$

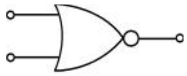
(C) $\left[\dfrac{\Delta V_{BB}}{\Delta I_B}\right]_{V_{BE}}$ (D) $\left[\dfrac{\Delta V_{BC}}{\Delta I_B}\right]_{V_{CE}}$

PART 8 : DIGITAL ELECTRONICS AND LOGIC GATES

Q.48 Which logic gate is represented by following diagram :



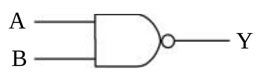
(A) AND (B) OR
(C) NOR (D) XOR

Q.49 Symbol  represents

(A) NAND gate (B) NOR gate
(C) NOT gate (D) XNOR gate

Q.50 The output of a NAND gate is 0 –
(A) If both inputs are 0.
(B) If one input is 0 and the other input is 1.
(C) If both inputs are 1
(D) Either if both inputs are 1 or if one of the inputs is 1 and the other 0

Q.51 Which gates is represented by this figure

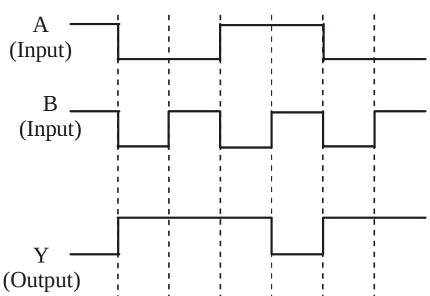


(A) NAND gate (B) AND gate
(C) NOT gate (D) OR gate

Q.52 Which of the following logic gate is an universal gate –
(A) OR (B) NOT
(C) AND (D) NOR

Q.53 The output of OR gate is 1
(A) If both inputs are zero.
(B) If either or both inputs are 1.
(C) Only if both input are 1.
(D) If either input is zero.

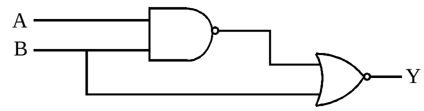
Q.54 Input and output waveforms are shown. Possible logic gate is –



(A) NAND gate (B) NOT gate
(C) OR gate (D) AND gate

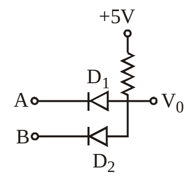
Q.55 In Boolean Algebra Y = A + B implies that –
(A) Output Y exists when both inputs A and B exist.
(B) Output Y exists when either input A exists or input B exists or both inputs A and B exist.
(C) Output Y exists when either input A exists or input B exists but not when both inputs A and B exist.
(D) Output Y exists when both inputs A and B exists but not when either input A or B exist.

Q.56 The output Y of the given gate combination is –



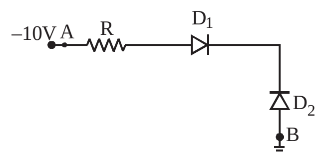
(A) 0 (B) 1
(C) $\overline{A}$ (D) $\overline{B}$

Q.57 Study the circuit shown in the figure. Name the gate that the given circuit resembles



(A) NAND (B) AND
(C) OR (D) NOR

Q.58 In Fig., assuming the diodes to be ideal,



(A) D_1 is forward biased and D_2 is reverse biased & hence current flows from A to B.
(B) D_2 is forward biased and D_1 is reverse biased and hence no current flows from B to A and vice versa.
(C) D_1 and D_2 are both forward biased and hence current flows from A to B.
(D) D_1 and D_2 are both reverse biased and hence no current flows from A to B and vice versa.

Q.59 Which of the following would produce digital signals?
(A) Musical sound
(B) A vibrating tuning fork.
(C) Sound and picture singals in TV
(D) Light pulse

EXERCISE - 2 (LEVEL-2)

Choose one correct response for each question.

Q.1 In a PN-junction diode –
(A) The current in the reverse biased condition is generally very small.
(B) The current in the reverse biased condition is small but the forward biased current is independent of the bias voltage.
(C) The reverse biased current is strongly dependent on the applied bias voltage.
(D) The forward biased current is very small in comparison to reverse biased current.

Q.2 The reverse biasing in a PN junction diode
(A) Decreases the potential barrier.
(B) Increases the potential barrier.
(C) Increases the number of minority charge carriers.
(D) Increases the number of majority charge carriers.

Q.3 In an NPN transistor the collector current is 24mA. If 80% of electrons reach collector its base current in mA is
(A) 36 (B) 26
(C) 16 (D) 6

Q.4 In a PNP transistor working as a common-base amplifier, current gain is 0.96 and emitter current is 7.2 mA. The base current is
(A) 0.4 mA (B) 0.2 mA
(C) 0.29 mA (D) 0.35 mA

Q.5 In a common emitter transistor, the current gain is 80. What is the change in collector current, when the change in base current is 250 μA
(A) $80 \times 250\ \mu A$ (B) $(250 - 80)\ \mu A$
(C) $(250 + 80)\ \mu A$ (D) $250/80\ \mu A$

Q.6 For a transistor the parameter β = 99. The value of the parameter α is
(A) 0.9 (B) 0.99
(C) 1 (D) 9

Q.7 In the CB mode of a transistor, when the collector voltage is changed by 0.5 volt. The collector current changes by 0.05 mA. The output resistance will be
(A) 10 kΩ (B) 20 kΩ
(C) 5 kΩ (D) 2.5 kΩ

Q.8 Consider an NPN transistor amplifier in common-emitter configuration. The current gain of the transistor is 100. If the collector current changes by 1 mA, what will be the change in emitter current
(A) 1.1 mA (B) 1.01 mA
(C) 0.01 mA (D) 10 mA

Q.9 If A and B are two inputs in AND gate, then AND gate has an output of 1 when the values of A and B are
(A) A = 0, B = 0 (B) A = 1, B = 1
(C) A = 1, B = 0 (D) A = 0, B = 1

Q.10 $\left(\dfrac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$ = ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at a constant base current I_B, is –
(A) input resistance (B) output resistance
(C) active resistance (D) passive resistance

Q.11 The truth-table given below is for which gate

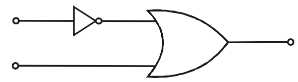
A	0	0	1	1
B	0	1	0	1
C	1	1	1	0

(A) XOR (B) OR
(C) AND (D) NAND

Q.12 In a transistor the current amplification factor is 0.98. If the given transistor is used in common emitter mode then the change in input current, corresponding to the change of 3.5 mA in output current, will be –
(A) 0.07 mA (B) 3.4 mA
(C) 3.57 mA (D) 171.5 mA

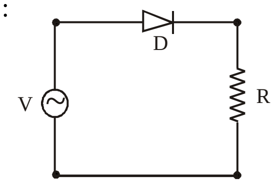
Q.13 In a transistor the current amplification factor α is 0.9. The transistor is connected in common base configuration. The change in collector current when base current changes by 4mA is –
(A) 4mA (B) 12mA
(C) 24mA (D) 36mA

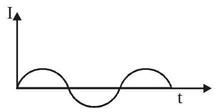
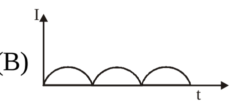
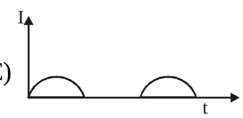
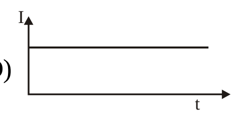
Q.14 The Boolean equation for the circuit given in figure is –



(A) $Y = A + \overline{B}$ (B) $Y = \overline{A + B}$
(C) $Y = \overline{A} + B$ (D) $Y = \overline{A} + \overline{B}$

Q.15 A p-n junction (D) shown in the figure can act as a rectifier. An alternating current source (V) is connected in the circuit. The current (I) in the resistor R can be shown by :



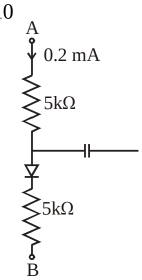
(A) 
(B) 
(C) 
(D) 

Q.16 In n-type semiconductor when all donor states are filled, then the net charge density in the donor states becomes
(A) 1 (B) > 1
(C) < 1,but not zero (D) zero

Q.17 Which of the following would produce analog signals
(A) A vibrating tuning fork. (B) Light pulse
(C) Output of NAND gate (D) All of these

Q.18 In pure semiconductor, the number of conduction electrons is 6×10^{18} per cubic metre. How many holes are there in a sample of size 1cm × 1 cm × 1 mm ?
(A) 3×10^{10} (B) 6×10^{11}
(C) 3×10^{11} (D) 6×10^{10}

Q.19 In the circuit shown in Fig., if the diode forward voltage drop is 0.3 V, the voltage difference between A and B is



(A) 1.3 V
(B) 2.3 V
(C) 0
(D) 0.5 V

Q.20 The following table provides the set of values of V and I obtained for a given diode. Let the characteristics curve be nearly linear, over this range, the forward and reverse bias resistance of the given diode respectively are –

	V	I
Forward biasing	2.0 V	60mA
	2.4 V	80mA
Reverse biasing	0 V	0 μA
	–2 V	–0.25 μA

(A) $10\ \Omega$, $8 \times 10^6\ \Omega$ (B) $20\ \Omega$, $4 \times 10^5\ \Omega$
(C) $20\ \Omega$, $8 \times 10^6\ \Omega$ (D) $10\ \Omega$, $10\ \Omega$

Q.21 Consider an npn transitor with its base-emitter junction forward biased and collector base junction reverse biased. Which of these are correct ?
I. Electrons cross over from emitter to collector.
II. Holes move from base to collector.
III. Electrons move from emitter to base.
IV. Electrons from emitter move out of base without going to the collector.
(A) I and III (B) I and II
(C) I and IV (D) II and III

Q.22 An oscillator is nothing but an amplifier with
(A) larger gain (B) positive feedback
(C) no feedback (D) negative feedback

Q.23 The conductivity of a semiconductor increases with increase in temperature because
(A) number density of free current carriers increases.
(B) relaxation time increases.
(C) both number density of carriers and relaxation time increase.
(D) number density of current carriers increases, relaxation time decreases but effect of decrease in relaxation time is much less than increase in number density.

Q.24 Which of the following statement is correct for an n-type semiconductor?
(A) The donor level lies below the bottom of the conduction band.
(B) The donor level lies closely above the top of the valence band.
(C) The donor level lies at the halfway mark of the forbidden energy gap.
(D) None of the above

Q.25 A pure Si crystal has 5×10^{22} atoms m^{-3}. It is doped by 1 ppm concentration of pentavalent As. The number of holes is $[n_i^2 = n_h n_e]$ (Take $n_i = 1.5 \times 10^{16}\ m^{-3}$)
(A) $4.5 \times 10^{9}\ m^{-3}$ (B) $4.5 \times 10^{6}\ m^{-3}$
(C) $2.5 \times 10^{9}\ m^{-3}$ (D) $2.5 \times 10^{6}\ m^{-3}$

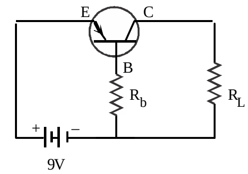
Q.26 To reduce the ripples in a rectifier circuit with capacitor filter
I. R_L should be increased.
II. input frequency should be decreased.
III. input frequency should be increased.
IV. capacitors with high capacitance should be used.
(A) I, II and III (B) I, III and IV
(C) II, III and IV (D) I, II and IV

Q.27 A p-n photo diode is made of a material with a band gap of 2eV. The minimum frequency of the radiation that can be absorbed by the material is nearly
(Take hc = 1240eV nm)
(A) 1×10^{14} Hz (B) 20×10^{14} Hz
(C) 10×10^{14} Hz (D) 5×10^{14} Hz

Q.28 Diffusion of electrons in unbiased p-n junction from n to p-side occurs due to
(A) potential difference.
(B) electric field attraction.
(C) breaking of semiconductor bonds.
(D) concentration gradient of electrons.

Q.29 In an unbiased p-n junction, holes diffuse from the p-region to n-region because –
(A) free electrons in the n-region attract them
(B) they move across the junction by the potential difference.
(C) hole concentration in p-region is more as compared to n-region.
(D) all of these

Q.30 In a transistor circuit shown here, the base current is 35μA. The value of resistance R_b



(A) 123.5 kΩ (B) 257 kΩ
(C) 380.05 kΩ (D) None of these

Q.31 Three photo diodes D_1, D_2 and D_3 are made of semiconductors having band gap of 2.5 eV, 2eV and 3eV, respectively. Which one will be able to detect light of wavelength 6000 Å ?
(A) D_1 (B) D_2
(C) D_3 (D) D_1 and D_2 both

Q.32 A photodetector is a
(A) photodiode used for detecting optical signals.
(B) LED's which are used for detection of infrared signals.
(C) an evacuated tube consisting of a photosensitive cathode.
(D) None of the above

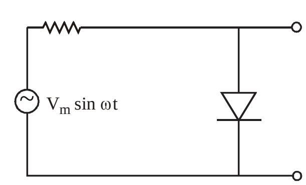
Q.33 If α and β are the current gain in the CB and CE configurations respectively of the transistor circuit, then

$$\frac{\beta - \alpha}{\alpha\beta} =$$

(A) zero (B) 1
(C) 2 (D) 0.5

Q.34 In an n-p-n transistor in CE configuration when V_{BE} is increased by small amount, then
(A) I_B increases & I_C increases proportionately
(B) I_B increases and I_C remains constant.
(C) I_B remains constant and I_C increases.
(D) both I_B and I_C remain nearly constant.

Q.35 The output of the given circuit in Fig.



(A) would be zero at all times.
(B) would be like a half wave rectifier with positive cycles in output.
(C) would be like a half wave rectifier with negative cycles in output.
(D) would be like that of a full wave rectifier.

Q.36 The colour of light emitted by a LED depends on
(A) its reverse bias
(B) the amount of forward current
(C) its forward bias
(D) type of semiconductor material

Q.37 Improper biasing of a transistor circuit produces
(A) heavy loading of emitter current
(B) distortion in the output signal
(C) excessive heat at collector terminal
(D) faulty location of load line

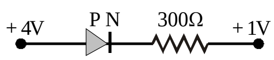
Q.38 An electrical device which offers a low resistance to the current in one direction but a high resistance to the current in opposite direction is
(A) current amplifier (B) oscillator
(C) power amplifier (D) rectifier

EXERCISE - 3 (NUMERICAL VALUE BASED QUESTIONS)

NOTE : The answer to each question is a NUMERICAL VALUE.

Q.1 How many NAND gates are used to form an AND gate.

Q.2 In the circuit given below, the value of the current is 10^{-X} amp. Find the value of X.



Q.3 A potential barrier of 0.50 V exists across a P-N junction. If the depletion region is 5.0×10^{-7}m wide, the intensity of the electric field in this region is 1.0×10^{X} V/m. Find the value of X.

Q.4 For a common base configuration of PNP transistor $\frac{I_C}{I_E} = 0.98$ then maximum current gain in common emitter configuration will be

Q.5 A common emitter amplifier is designed with NPN transistor ($\alpha = 0.99$). The input impedance is 1 KΩ and load is 10 KΩ. The voltage gain will be $(110 \times X)$. Find the value of X.

Q.6 How many AM broadcast stations can be accommodated in a 100 kHz bandwidth if the highest frequency modulating a carrier is 5 kHz ?

Q.7 An audio signal is given by 30 sin $(2\pi \times 2000t)$ is used for modulating a carrier wave given by the equation 60 sin $(2\pi \times 200000t)$, find the percentage modulation.

EXERCISE - 4 [PREVIOUS YEARS JEE MAIN QUESTIONS]

Q.1 If temperature increases, conductivity of semiconductor will be - **[AIEEE-2002]**
(A) increases (B) decreases
(C) remain unchanged (D) none of these

Q.2 At 0K, silicon behave as – **[AIEEE-2002]**
(A) super conductor (B) conductor
(C) Insulator (D) none of these

Q.3 The energy band gap is maximum in – **[AIEEE-2002]**
(A) Metals (B) Superconductors
(C) Insulators (D) Semiconductors

Q.4 The part of a transistor which is most heavily doped to produce large number of majority carriers is
(A) Emitter **[AIEEE-2002]**
(B) Base
(C) Collector
(D) Can be any of the above three

Q.5 In the middle of the depletion layer of a reverse-biased p-n junction, the – **[AIEEE-2003]**
(A) Potential is maximum
(B) Electric field is maximum
(C) Potential is zero
(D) Electric field is zero

Q.6 The difference in the variation of resistance with temperature in a metal and a semiconductor arises essentially due to the difference in the – **[AIEEE-2003]**
(A) Variation of the number of charge carriers with temperature.
(B) Type of bonding
(C) Variation of scattering mechanism with temperature
(D) Crystal structure

Q.7 A strip of copper and another of germanium are cooled from room temperature of 80 K. The resistance of –
(A) copper strip increases and that of germanium decreases. **[AIEEE-2003]**
(B) copper strip decreases and that of germanium increases.
(C) each of these increases
(D) each of these decreases

Q.8 When npn transistor is used as an amplifier –
(A) electrons move from collector base. **[AIEEE-2004]**
(B) holes move from emitter to base
(C) electrons move from base to collector
(D) holes move from base to emitter

Q.9 A piece of copper and another of germanium are cooled from room temperature of 77 K, the resistance of –
(A) copper increases and germanium. **[AIEEE-2004]**
(B) each of them decreases.
(C) each of these increases.
(D) copper decreases and germanium increases

Q.10 The manifestation of band structure in solids is due to –
(A) Bohr's correspondence principle **[AIEEE-2004]**
(B) Pauli's exclusion principle
(C) Heisenberg's uncertainty principle
(D) Boltzmann's law

Q.11 When p–n junction diode is forward biased, then –
(A) both the depletion region and barrier height are reduced. **[AIEEE-2004]**
(B) the depletion region is widened and barrier height is reduced.
(C) the depletion region is reduced and barrier height is increased.
(D) both the depletion region and barrier height are increased.

Q.12 The electrical conductivity of a semiconductor increases when electromagnetic radiation of wavelength shorter than 2480 nm is incident on it. The band gap in (eV) for the semiconductor is **[AIEEE-2005]**
(A) 1.1 eV (B) 2.5 eV
(C) 0.5 eV (D) 0.7 eV

Q.13 In a full wave rectifier circuit operating from 50 Hz mains frequency, the fundamental frequency in the ripple would be **[AIEEE-2005]**
(A) 50 Hz (B) 25 Hz
(C) 100 Hz (D) 70.7 Hz

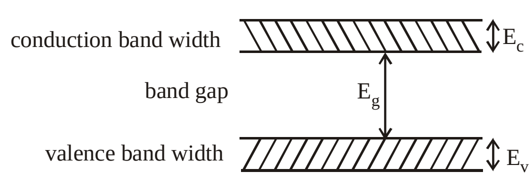
Q.14 In a common base amplifier the phase difference between the input signal voltage and output voltage is
(A) $\pi/4$ (B) π **[AIEEE-2005]**
(C) 0 (D) $\pi/2$

Q.15 If the ratio of the concentration of electrons to that of holes in a semiconductor is 7/5and the ratio of currents is 7/4, then what is the ratio of their drift velocities –
(A) 5/4 (B) 4/7 **[AIEEE 2006]**
(C) 5/8 (D) 4/5

Q.16 A solid which is not transparent to visible light and whose conductivity increases with temperature is formed by – **[AIEEE 2006]**
(A) Vander Waals binding (B) Metallic binding
(C) Ionic binding (D) Covalent binding

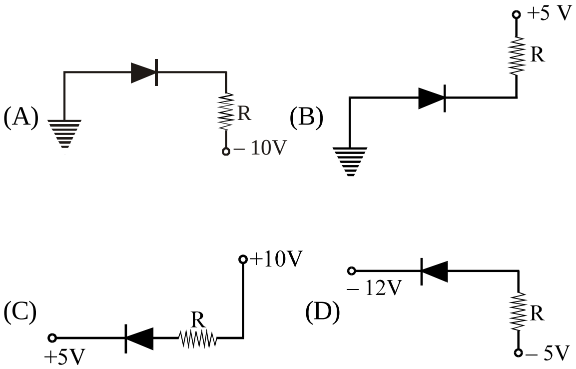
Q.17 In a common base mode of a transistor, the collector current is 5.488 mA for an emitter current of 5.60 mA. The value of the base current amplification (β) will be –
(A) 51 (B) 48 **[AIEEE 2006]**
(C) 49 (D) 50

Q.18 If the lattics constant of this semiconductor is decreased, then which of the following is correct – **[AIEEE 2006]**

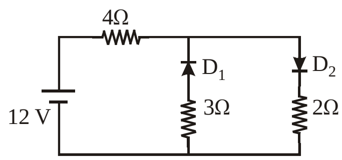


(A) E_c and E_v decrease, but E_g increases
(B) All E_c, E_g, E_v decrease
(C) All E_c, E_g, E_v increase
(D) E_c and E_v increase, but E_g decreases

Q.19 In the following, which one of the diodes is reverse biased **[AIEEE 2006]**

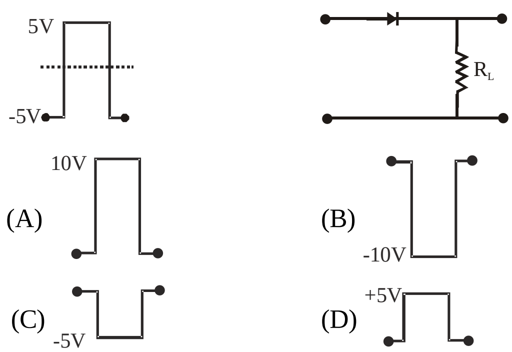


Q.20 The circuit has two oppositely connected ideal diodes in parallel. What is the current flowing in the circuit ? **[AIEEE 2006]**



(A) 2.31 A (B) 1.33 A
(C) 1.71 A (D) 2.00 A

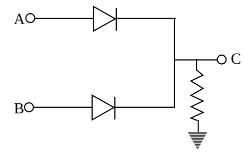
Q.21 If in a p-n junction diode, a square input signal of 10V is applied as shown. Then the output signal across R_L will be **[AIEEE 2007]**



Q.22 Carbon, silicon and germanium have four valence electrons each. At room temperature which one of the following statements is most appropriate ?**[AIEEE 2007]**
(A) The number of free conduction electrons is significant in C but small in Si and Ge.
(B) The number of free conduction electrons is negligibly small in all the three.
(C) The number of free electrons for conduction is significant in all the three.
(D) The number of free electrons for conduction is significant only in Si and Ge but small in C.

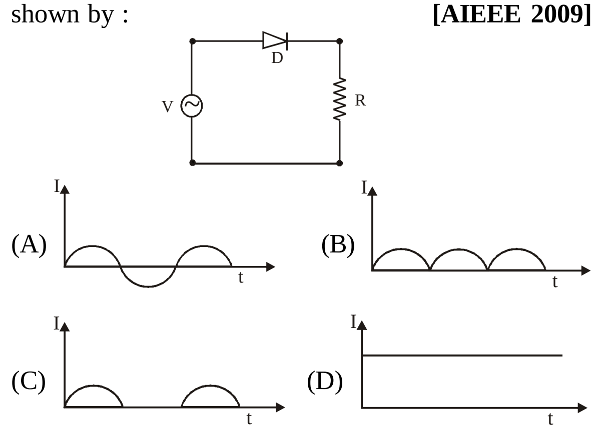
Q.23 A working transistor with its three legs marked P, Q and R is tested using a multimeter. No conduction is found between P and Q. By connecting the common (negative) terminal of the multimeter to R and the other (positive) terminal to P or Q, some resistance is seen on the multimeter. Which of following is true for the transistor **[AIEEE 2008]**
(A) It is a pnp transistor with R as collector
(B) It is a pnp transistor with R as emitter
(C) It is an npn transistor with R as collector
(D) It is an npn transistor with R as base

Q.24 In the circuit below, A and B represent two inputs and C represents the output. **[AIEEE 2008]**

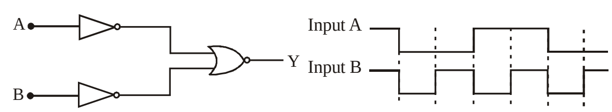


The circuit represents
(A) AND gate (B) NAND gate
(C) OR gate (D) NOR gate

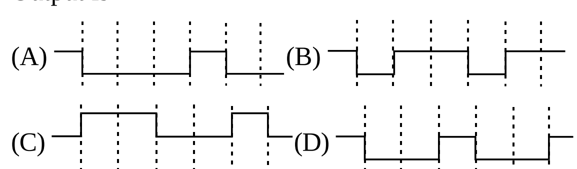
Q.25 An p-n junction (D) shown in the figure can act as a rectifier. An alternating current source (V) is connected in the circuit. The current (I) in the resistor R can be shown by : **[AIEEE 2009]**



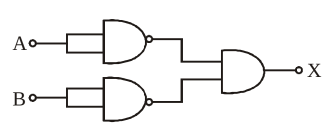
Q.26 The logic circuit shown below has the input waveforms 'A' and 'B' as shown. Pick out the corret output waveform. **[AIEEE 2009]**



Output is -



Q.27 The combination of gates shown below yields **[AIEEE 2010]**



(A) OR gate (B) NOT gate
(C) XOR gate (D) NAND gate

Q.28 **Statement-1 :** Skywave signals are used for long distance radio communication. These signals are in general, less stable than ground wave signals. **[AIEEE 2011]**

Statement-2 : The state of ionosphere varies from hour to hour, day to day and season to season.

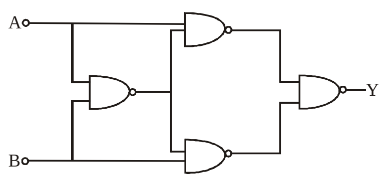
(A) Statement-1 is true, statement-2 is false.

(B) Statement-1 is true, Statement-2 is true, Statement-2 is the correct explanation of Statement-1.

(C) Statement-1 is true, Statement-2 is true, Statement-2 is not the correct explanation of Statement-1.

(D) Statement-1 is false, Statement-2 is true.

Q.29 Truth table for system of four NAND gates as shown in figure is : **[AIEEE 2012]**



(A)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(B)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

(C)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

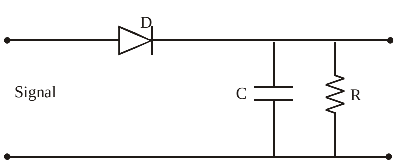
(D)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Q.30 A radar has a power of 1 kW and is operating at a frequency of 10 GHz. It is located on a mountain top of height 500m. The maximum distance upto which it can detect object located on the surface of the earth (Radius of earth = 6.4×10^6 m) is : **[AIEEE 2012]**

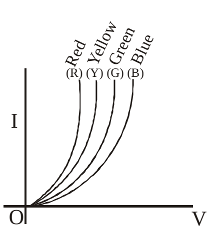
(A) 80 km (B) 16 km
(C) 40 km (D) 64 km

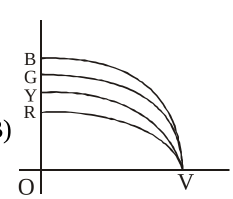
Q.31 A diode detector is used to detect an amplitude modulated wave of 60% modulation by using a condenser of capacity 250 pico farad in parallel with a load resistance 100 kilo ohm. Find the maximum modulated frequency which could be detected by it – **[JEE MAIN 2013]**

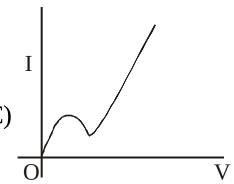


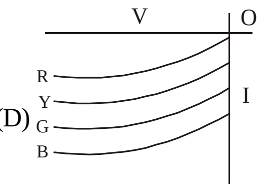
(A) 10.62 MHz (B) 10.62 kHz
(C) 5.31 MHz (D) 5.31 kHz

Q.32 The I–V characteristic of an LED is – **[JEE MAIN 2013]**

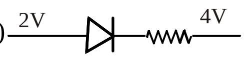
(A) 

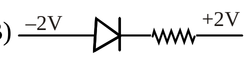
(B) 

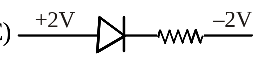
(C) 

(D) 

Q.33 The forward biased diode connection is **[JEE MAIN 2014]**

(A) 

(B) 

(C) 

(D) 

Q.34 A signal of 5 kHz frequency is amplitude modulated on a carrier wave of frequency 2 MHz. The frequencies of the resultant signal is/are **[JEE MAIN 2015]**

(A) 2005 kHz and 1995 kHz
(B) 2005 kHz, 2000 kHz and 1995 kHz
(C) 2000 kHz and 1995 kHz
(D) 2 MHz only

Q.35 The temperature dependence of resistances of Cu and undoped Si in the temperature range 300-400K, is best described by: **[JEE MAIN 2015]**

(A) Linear increase for Cu, exponential increase for Si
(B) Linear increase for Cu, exponential decrease for Si
(C) Linear decrease for Cu, linear decrease for Si
(D) Linear increase for Cu, linear increase for Si

Q.36 Choose the correct statement: **[JEE MAIN 2015]**

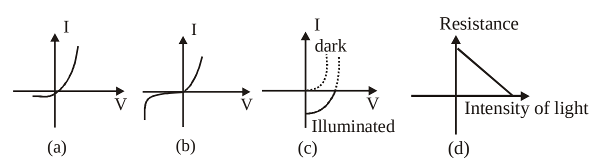
(A) In amplitude modulation the frequency of the high frequency carrier wave is made to vary in proportion to the amplitude of the audio signal.

(B) In frequency modulation the amplitude of the high frequency carrier wave is made to vary in proportion to the amplitude of the audio signal.

(C) In frequency modulation the amplitude of the high frequency carrier wave is made to vary in proportion to the frequency of the audio signal.

(D) In amplitude modulation the amplitude of the high frequency carrier wave is made to vary in proportion to the amplitude of the audio signal.

Q.37 Identify the semiconductor devices whose characteristics are in the order (1), (2), (3), (4): **[JEE MAIN 2016]**



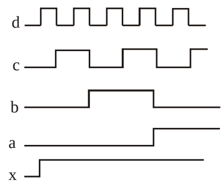
(A) Zener diode, Simple diode, Light dependent resistance, Solar cell.

(B) Solar cell, Light dependent resistance, Zener diode, Simple diode.

(C) Zener diode, solar cell, Simple diode, Light dependent resistance.

(D) Simple diode, Zener diode, Solar cell, Light dependent resistance.

Q.38 If a, b, c, d are inputs to a gate and x is its output, then, as per the following time graph, the gate is: **[JEE MAIN 2016]**



(A) AND (B) OR
(C) NAND (D) NOT

Q.39 For a common emitter configuration, if α and β have their usual meanings, the incorrect relationship between α & β **[JEE MAIN 2016]**

(A) $\alpha = \frac{\beta}{1-\beta}$ (B) $\alpha = \frac{\beta}{1+\beta}$ (C) $\alpha = \frac{\beta^2}{1+\beta^2}$ (D) $\frac{1}{\alpha} = \frac{1}{\beta} + 1$

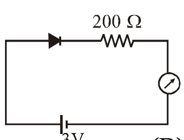
Q.40 In amplitude modulation, sinusoidal carrier frequency used is denoted by ω_c and the signal frequency is denoted by ω_m. The bandwidth ($\Delta\omega_m$) of the signal is such that $\Delta\omega_m << \omega_c$. Which of the following frequencies is not contained in the modulated wave? **[JEE MAIN 2017]**

(A) ω_c (B) $\omega_m + \omega_c$
(C) $\omega_c - \omega_m$ (D) ω_m

Q.41 In a common emitter amplifier circuit using an n-p-n transistor, the phase difference between the input and the output voltages will be: **[JEE MAIN 2017]**

(A) 90º (B) 135º
(C) 180º (D) 45º

Q.42 The reading of the ammeter for a silicon diode in the given circuit is: **[JEE MAIN 2018]**



(A) 11.5 mA (B) 13.5 mA
(C) 0 (D) 15 mA

Q.43 A telephonic communication service is working at carrier frequency of 10 GHz. Only 10% of it is utilized for transmission. How many telephonic channels can be transmitted simultaneously if each channel requires a band width of 5 kHz? **[JEE MAIN 2018]**

(A) 2×10^5 (B) 2×10^6
(C) 2×10^3 (D) 2×10^4

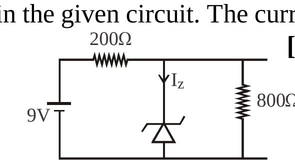
Q.44 Mobility of electrons in a semiconductor is defined as the ratio of their drift velocity to the applied electric field. If, for an n-type semiconductor, the density of electrons is 10^{19} m^{-3} and their mobility is 1.6 $m^2/(V.s)$ then the resistivity of the semi-conductor (since it is an n-type semiconductor contribution of holes is ignored) is close to: **[JEE MAIN 2019 (JAN]**

(A) 2 Ωm (B) 0.4 Ωm
(C) 4 Ωm (D) 0.2 Ωm

Q.45 In a communication system operating at wavelength 800 nm, only one percent of source frequency is available as signal bandwidth. The number of channels accomodated for transmitting TV signals of band width 6 MHz are (Take velocity of light $c = 3 \times 10^8$ m/s, $h = 6.6 \times 10^{-34}$ J-s) **[JEE MAIN 2019 (JAN)]**

(A) 3.75×10^6 (B) 4.87×10^5
(C) 3.86×10^6 (D) 6.25×10^5

Q.46 The reverse breakdown voltage of a Zener diode is 5.6 V in the given circuit. The current I_Z through the Zener is **[JEE MAIN 2019 (APRIL)]**

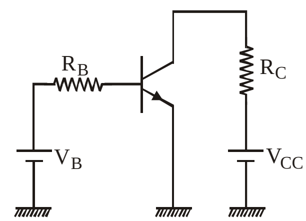


(A) 7 mA (B) 17 mA
(C) 10 mA (D) 15 mA

Q.47 The wavelength of the carrier waves in a modern optical fiber communication network is close to : **[JEE MAIN 2019 (APRIL)]**

(A) 600 nm (B) 900 nm
(C) 2400 nm (D) 1500 nm

Q.48 A common emitter amplifier circuit, built using an npn transistor, is shown in the figure. Its dc current gain is 250, $R_C = 1k\Omega$ and $V_{CC} = 10V$. What is the minimum base current for V_{CE} to reach saturation ? **[JEE MAIN 2019 (APRIL)]**

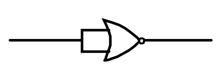
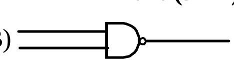


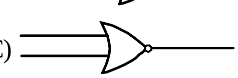
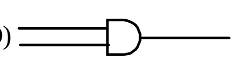
(A) 100 μA (B) 7 μA
(C) 40 μA (D) 10 μA

Q.49 In a line of sight radio communication, a distance of about 50 km is kept between the transmitting and receiving antennas. If the height of the receiving antenna is 70m, then the minimum height of the transmitting antenna should be : **[JEE MAIN 2019 (APRIL)]**
(Radius of the Earth = 6.4×10^6 m).

(A) 40 m (B) 51 m
(C) 32 m (D) 20 m

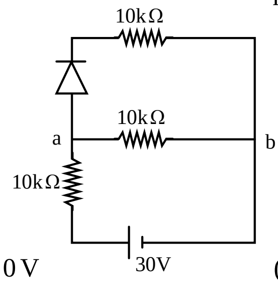
Q.50 Which of the following gives a reversible operation? **[JEE MAIN 2020 (JAN)]**

(A)  (B) 

(C)  (D) 

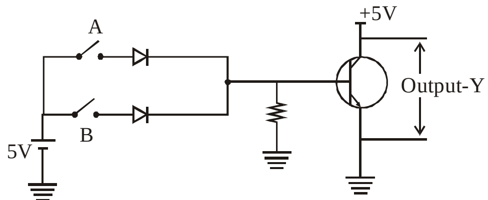
Q.51 There is a electric circuit as shown in the figure. Find potential difference between points a and b.

[JEE MAIN 2020 (JAN)]



(A) 0 V (B) 15 V
(C) 10 V (D) 5 V

Q.52 Boolean relation at the output stage-Y for the following circuit is : **[JEE MAIN 2020 (JAN)]**

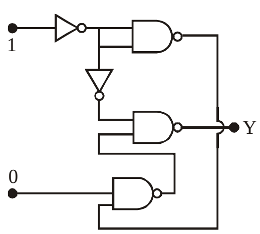


(A) A + B (B) $\overline{A}+\overline{B}$

(C) $\overline{A}\cdot\overline{B}$ (D) A · B

Q.53 In the given circuit, value of Y is :

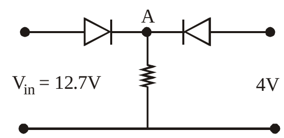
[JEE MAIN 2020 (JAN)]



(A) will not execute (B) 0
(C) toggles between 0 and 1 (D) 1

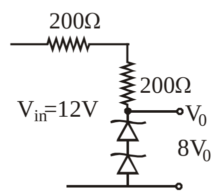
Q.54 Both the diodes used in the circuit shown are assumed to be ideal and have negligible resistance when these are forward biased. Built in potential in each diode is 0.7V. For the input voltages shown in the figure, the voltage (in Volts) at point A is _______.

[JEE MAIN 2020 (JAN)]



Q.55 The circuit shown below is working as a 8 V dc regulated voltage source. When 12 V is used as input, the power dissipated (in mW) in each diode is; (considering both zener diodes are identical) _________.

[JEE MAIN 2020 (JAN)]



EXERCISE - 5 [PREVIOUS YEARS AIPMT / NEET QUESTIONS]

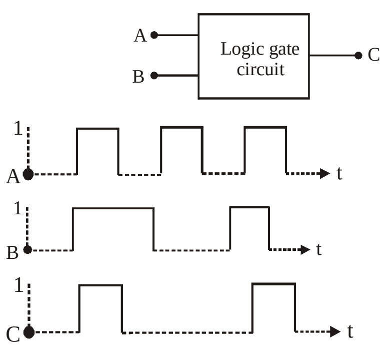
Q.1 Choose the only false statement from the following –
(A) In conductors, the valence and conduction band may overlap. **[AIPMT 2005]**
(B) Substances with energy gap of the order of 10eV are insulators.
(C) The resistivity of a semiconductor increases with increase in temperature.
(D) The conductivity of a semiconductor increases with increase in temperature.

Q.2 Carbon, silicon and germanium atoms have four valence electrons each. Their valence and conduction bands are separated by energy band gaps respresented by $(E_g)_C$, $(E_g)_{Si}$ and $(E_g)_{Ge}$ respectively. Which one of the following relationships is true in their case ? **[AIPMT 2005]**
(A) $(E_g)_C > (E_g)_{Si}$ (B) $(E_g)_C < (E_g)_{Si}$
(C) $(E_g)_C = (E_g)_{Si}$ (D) $(E_g)_C < (E_g)_{Ge}$

Q.3 Application of a foward bias to a p-n junction –
(A) widens the depletion zone. **[AIPMT 2005]**
(B) increases the potential difference across the depletion zone.
(C) increases the number of donors on the n side.
(D) increases the electric field in the depletion zone.

Q.4 Zener diode is used for – **[AIPMT 2005]**
(A) Amplification
(B) Rectification
(C) Stabilisation
(D) Producing oscillations in an oscillator

Q.5 The following figure shows a logic gate circuit with two inputs A and B and the output C. The voltage wavefronts of A, B and C are as shown below. The logic circuit gate is **[AIPMT 2006]**



(A) NAND gate (B) NOR gate
(C) OR gate (D) AND gate

Q.6 A transistor is operated in common emitter configuration at constant collector voltage V_C = 1.5V such that a change in the base current from 100μA to 150μA produces a change in the collector current from 5mA to 10mA. The current gain (β) is – **[AIPMT 2006]**
(A) 75 (B) 100
(C) 50 (D) 67

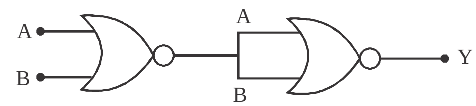
Q.7 A forward biased diode is – **[AIPMT 2006]**
(A) 

(B) 

(C) 

(D) 

Q.8 In the following circuit, the output Y for all possible inputs A and B is expressed by the truth table **[AIPMT 2007]**



(A)

A	B	Y
0	1	1
0	1	1
1	0	1
1	1	0

(B)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

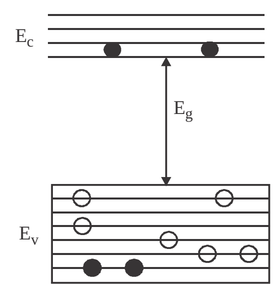
(C)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(D)

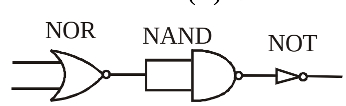
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Q.9 In the energy band diagram of a material shown, the open circles and filled circles denote holes & electrons respectively. The material is **[AIPMT 2007]**



(A) an insulator
(B) a metal
(C) an n-type semiconductor
(D) a p-type semiconductor

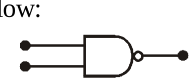
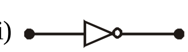
Q.10 The voltage gain of an amplifier with 9% negative feedback is 10.The voltage gain without feedback will be
(A) 100 (B) 90 **[AIPMT 2008]**
(C) 10 (D) 1.25

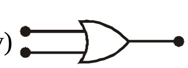
Q.11 The circuit 

is equivalent to – **[AIPMT 2008]**
(A) OR gate (B) AND gate
(C) NAND gate (D) NOR gate

Q.12 A p-n photodiode is made of a material with a band gap of 2.0 eV. The minimum frequency of the radiation that can be absorbed by the material is nearly **[AIPMT 2008]**
(A) 20×10^{14} Hz (B) 10×10^{14} Hz
(C) 5×10^{14} Hz (D) 1×10^{14} Hz

Q.13 The symbolic representation of four logic gates are given below:

(i)  (ii) 

(iii)  (iv) 

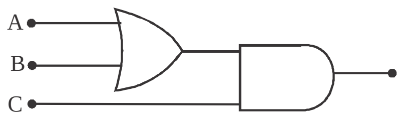
The logic symbols for OR, NOT and NAND gates are respectively: **[AIPMT 2009]**

(A) (iv), (i), (iii) (B) (iv), (ii), (i)
(C) (i), (iii), (iv) (D) (iii), (iv), (ii)

Q.14 A p-n photodiode is fabricated from a semiconductor with a band gap of 2.5eV. It can detect a signal of wavelength: **[AIPMT 2009]**
(A) 4000 nm (B) 6000 nm
(C) 4000 Å (D) 6000 Å

Q.15 A transistor is operated in common-emitter configuration at V_C = 2V such that a change in the base current from 100μA to 200μA produces a change in the collector current from 5 mA to 10 mA. The current gain is: **[AIPMT 2009]**
(A) 100 (B) 150
(C) 50 (D) 75

Q.16 To get an output Y = 1 from the circuit shown below the input must be **[AIPMT (PRE) 2010]**



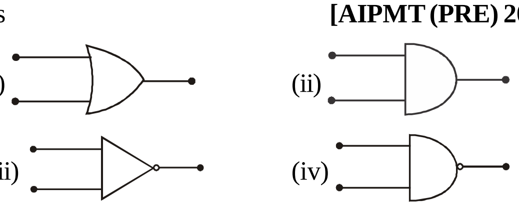
	A	B	C		A	B	C
(A)	0	1	0	(B)	0	0	1
(C)	1	0	1	(D)	1	0	0

Q.17 A common emitter amplifier has a voltage gain of 50, an .... Ω and an output impedance of 200Ω. The power gain of the amplifier is – **[AIPMT (PRE) 2010]**
(A) 500 (B) 1000
(C) 1250 (D) 50

Q.18 Which one of the following statement is false? **[AIPMT (PRE) 2010]**
(A) Pure Si doped with trivalent impurities gives a p-type semiconductor.
(B) Majority carriers in a n-type semiconductor are holes.
(C) Minority carriers in a p-type semiconductor are electrons.
(D) The resistance of intrinisic semiconductor decreases with increase of temperature.

Q.19 The device that acts as a complete electronic circuit is – **[AIPMT (PRE) 2010]**
(A) junction diode (B) integrated circuit
(C) junction transistor (D) zener diode

Q.20 Symbolic representation of four logic gates are shown as **[AIPMT (PRE) 2011]**

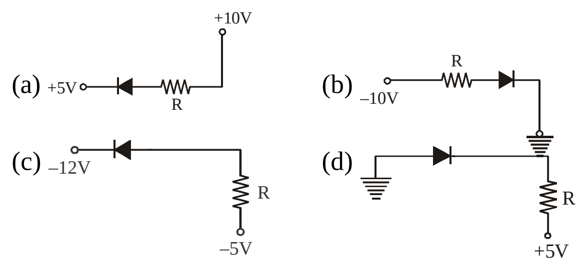


Pick out which ones are for AND, NAND and NOT gates, respectively :
(A) (ii), (iv) and (iii) (B) (ii), (iii) and (iv)
(C) (iii), (ii) and (i) (D) (iii), (ii) and (iv)

Q.21 If a small amount of antimony is added to germanium crystal– **[AIPMT (PRE) 2011]**
(A) Its resistance is increased.
(B) It becomes a p-type semiconductor.
(C) The antimony becomes an acceptor atom.
(D) There will be more free electrons than hole in the semiconductor.

Q.22 In forward biasing of the p-n junction **[AIPMT (PRE) 2011]**
(A) The positive terminal of the battery is connected to p-side and the depletion region becomes thin.
(B) The positive terminal of the battery is connected to p-side and the depletion region becomes thick.
(C) The positive terminal of the battery is connected to n-side and the depletion region becomes thin.
(D) The positive terminal of the battery is connected to n-side and the depletion region becomes thick.

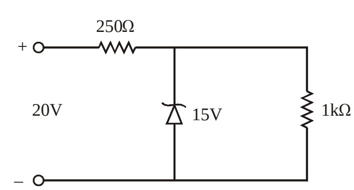
Q.23 In the following figure, the diodes which are forward biased, are **[AIPMT (MAINS) 2011]**



(A) (c) only (B) (c) and (a)
(C) (b) and (d) (D) (a), (b) and (d)

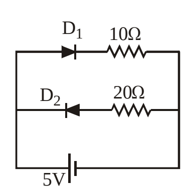
Q.24 Pure Si at 500K has equal number of electron (n_e) and hole (n_h) concentrations of 1.5×10^{16} m^{-3}. Doping by indium increases n_h to 4.5×10^{22} m^{-3}. The doped semiconductor is of : **[AIPMT (MAINS) 2011]**
(A) n-type with electron concentration $n_e = 5\times10^{22}$ m^{-3}
(B) p-type with electron concentration $n_e = 2.5\times10^{10}$ m^{-3}
(C) n-type with electron concentration $n_e = 2.5\times10^{23}$ m^{-3}
(D) p-type having electron concentrations $n_e = 5\times10^{9}$ m^{-3}

Q.25 A zener diode, having breakdown voltage equal to 15V, is used in a voltage regulator circuit shown in figure. The current through the diode is **[AIPMT (MAINS) 2011]**



(A) 10mA (B) 15 mA
(C) 20 mA (D) 5 mA

Q.26 Two ideal diodes are connected to a battery as shown in the circuit. The current supplied by the battery is – **[AIPMT (PRE) 2012]**

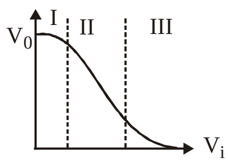


(A) 0.75 A (B) zero
(C) 0.25 A (D) 0.5 A

Q.27 In a CE transistor amplifier, the audio signal voltage .... Ω is 2V. If the base resistance is 1kΩ and the current amplification of the transistor is 100, the input signal voltage is **[AIPMT (PRE) 2012]**

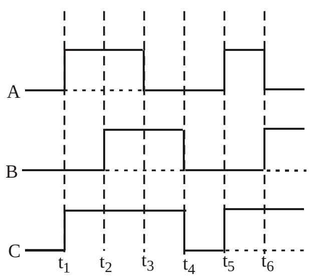
(A) 0.1 V (B) 1.0 V
(C) 1mV (D) 10mV

Q.28 Transfer characteristics [output voltage (V_0) vs input voltage (V_i)] for a base biased transistor in CE configuration is as shown in the figure. For using transistor as a switch, it is used : **[AIPMT (PRE) 2012]**



(A) in region III (B) both in region (I) & (III)
(C) in region II (D) in region I

Q.29 The figure shows a logic circuit with two inputs A and B and the output C. The voltage wave forms across A, B and C are as given. The logic circuit gate is : **[AIPMT (PRE) 2012]**



(A) OR gate (B) NOR gate
(C) AND gate (D) NAND gate

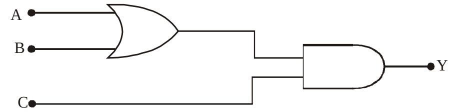
Q.30 C and Si both have same lattice structure, having 4 bonding electrons in each. However, C is insulator where as Si is intrinsic semiconductor. This is because – **[AIPMT (PRE) 2012]**

(A) In case of C the valence band is not completely filled at absolute zero temperature.
(B) In case of C the conduction band is partly filled even at absolute zero temperature.
(C) The four bonding electrons in the case of C lie in the second orbit, whereas in the case of Si they lie in the third.
(D) The four bonding electrons in the case of C lie in the third orbit, whereas for Si they lie in the fourth orbit.

Q.31 The input resistance of a silicon transistor is 100Ω. Base current is changed by 40 μA which results in a change in collector current by 2mA. This transistor is used as a common emitter amplifier with a load resistance of 4 KΩ. The voltage gain of the amplifier is : **[AIPMT (MAINS) 2012]**

(A) 2000 (B) 3000
(C) 4000 (D) 1000

Q.32 To get an output Y = 1 in given circuit which of the following input will be correct : **[AIPMT (MAINS) 2012]**

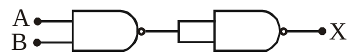


	A	B	C		A	B	C
(A)	1	0	0	(B)	1	0	1
(C)	1	1	0	(D)	0	1	0

Q.33 In a common emitter (CE) amplifier having a voltage gain G, the transistor used has transconductance 0.03 mho and current gain 25. If the above transistor is replaced with another one with transconductance 0.02 mho and current gain 20, the voltage gain will be **[NEET 2013]**

(A) (5/4) G (B) (2/3) G
(C) 1.5 G (D) (1/3) G

Q.34 The output (X) of the logic circuit shown in figure will be **[NEET 2013]**



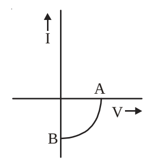
(A) $X = \overline{A + B}$ (B) $X = \overline{\overline{A}} . \overline{\overline{B}}$

(C) $X = \overline{A.B}$ (D) $X = A . B$

Q.35 In a n-type semiconductor, which of the following statement is true: **[NEET 2013]**

(A) Holes are majority carriers and trivalent atoms are dopants.
(B) Electrons are majority carriers and trivalent atoms are dopants.
(C) Electron are minority carriers and pantavalent atoms are dopants.
(D) Holes are minority carriers and pentavalent atoms are dopants.

Q.36 The given graph represents V-I characteristic for a semiconductor device. Which of the following statement is correct? **[AIPMT 2014]**

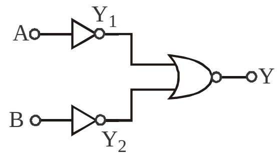


(A) It is V – I characteristic for solar cell where point A represents open circuit voltage and point B short circuit current.
(B) It is for a solar cell and points A and B represent open circuit voltage and current, respectively.
(C) It is for a photodiode and points A and B represent open circuit voltage and current, respectively.
(D) It is for a LED and points A and B represents open circuit voltage and short circuit current respectively.

Q.37 The barrier potential of a p-n junction depends
a. Type of semiconductor material
b. Amount of doping
c. Temperature **[AIPMT 2014]**
Which one of the following is correct?

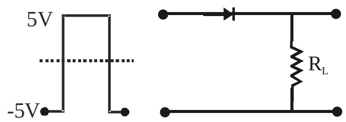
(A) a and b only (B) b only
(C) b and c only (D) a, b and c

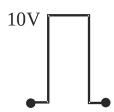
Q.38 Which logic gate is represented by the following combination of logic gate? **[AIPMT 2015]**

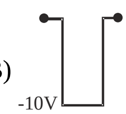


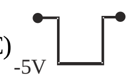
(A) NAND (B) AND
(C) NOR (D) OR

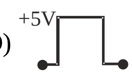
Q.39 If in a p-n junction a square input signal of 10V is applied, as shown, then the output across R_L will be **[AIPMT 2015]**



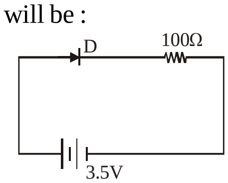
(A) 

(B) 

(C) 

(D) 

Q.40 In the given figure, a diode D is connected to an external resistance R = 100 Ω and an e.m.f of 3.5V. If the barrier potential developed across the diode is 0.5 V, the current in the circuit will be : **[RE-AIPMT 2015]**



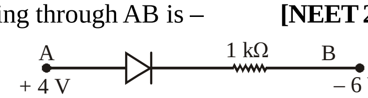
(A) 35 mA (B) 30 mA
(C) 40 mA (D) 20 mA

Q.41 The input signal given to a CE amplifier having a voltage gain of 150 is $V_i = 2\cos\left(15t + \frac{\pi}{3}\right)$. The corresponding output signal will be – **[RE-AIPMT 2015]**

(A) $300\cos\left(15t + \frac{4\pi}{3}\right)$ (B) $300\cos\left(15t + \frac{\pi}{3}\right)$

(C) $75\cos\left(15t + \frac{2\pi}{3}\right)$ (D) $2\cos\left(15t + \frac{5\pi}{6}\right)$

Q.42 Consider the junction diode as ideal. The value of current flowing through AB is – **[NEET 2016 PHASE 1]**

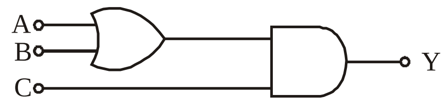


(A) 0 A (B) 10^{-2} A
(C) 10^{-1} A (D) 10^{-3} A

Q.43 A npn transistor is connected in common emitter configuration in a given amplifier. A load resistance of 800Ω is connected in the collector circuit and the voltage drop across it is 0.8 V. If the current amplification factor is 0.96 and the input resistance of the circuit is 192 Ω, the voltage gain and the power gain of the amplifier will respectively be – **[NEET 2016 PHASE 1]**

(A) 4, 3.84 (B) 3.69, 3.84
(C) 4, 4 (D) 4, 3.69

Q.44 To get output 1 for the following circuit, the correct choice for the input is – **[NEET 2016 PHASE 1]**

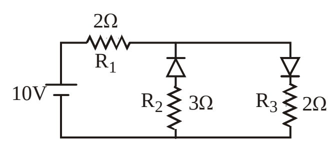


(A) A = 0, B = 1, C = 0 (B) A = 1, B = 0, C = 0
(C) A = 1, B = 1, C = 0 (D) A = 1, B = 0, C = 1

Q.45 For CE transistor amplifier, the audio signal voltage across the collector resistance of 2 kΩ is 4 V. If the current amplification factor of the transistor is 100 and the base resistance is 1kΩ, then the input signal voltage is **[NEET 2016 PHASE 2]**

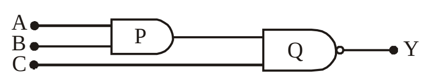
(A) 10 mV (B) 20 mV
(C) 30 mV (D) 15 mV

Q.46 The given circuit has two ideal diodes connected as shown in the figure below. The current flowing through the resistance R_1 will be – **[NEET 2016 PHASE 2]**



(A) 2.5 A (B) 10.0 A
(C) 1.43 A (D) 3.13 A

Q.47 What is the output Y in the following circuit, when all the three inputs A, B, C are first 0 and then 1? **[NEET 2016 PHASE 2]**

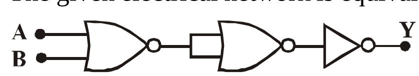


(A) 0, 1 (B) 0, 0
(C) 1, 0 (D) 1, 1

Q.48 In a common emitter transistor amplifier the audio signal voltage across the collector is 3V. The resistance of collector is 3 kΩ. If current gain is 100 and the base resistance is 2kΩ, the voltage and power gain of the amplifier is **[NEET 2017]**

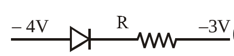
(1) 15 and 200 (2) 150 and 15000
(3) 20 and 2000 (4) 200 and 1000

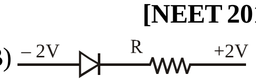
Q.49 The given electrical network is equivalent to : **[NEET 2017]**

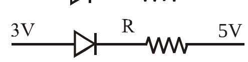


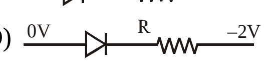
(A) OR gate (B) NOR gate
(C) NOT gate (D) AND gate

Q.50 Which one of the following represents forward bias diode? **[NEET 2017]**

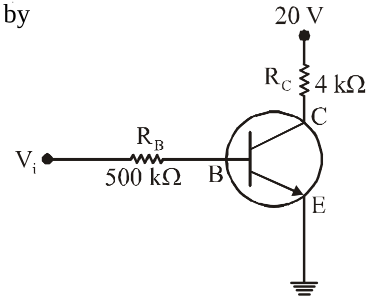
(A) 

(B) 

(C) 

(D) 

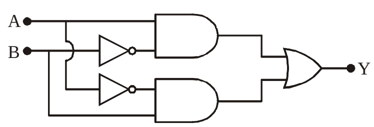
Q.51 In the circuit shown in the figure, the input voltage V_i is 20V, $V_{BE} = 0$ and $V_{CE} = 0$. The values of I_B, I_C and β are given by **[NEET 2018]**



(A) $I_B = 20\ \mu A$, $I_C = 5$ mA, $\beta = 250$
(B) $I_B = 25\ \mu A$, $I_C = 5$ mA, $\beta = 200$
(C) $I_B = 40\ \mu A$, $I_C = 10$ mA, $\beta = 250$
(D) $I_B = 40\ \mu A$, $I_C = 5$ mA, $\beta = 125$

Q.52 In a p-n junction diode, change in temperature due to heating **[NEET 2018]**
(A) Does not affect resistance of p-n junction.
(B) Affects only forward resistance.
(C) Affects only reverse resistance.
(D) Affects the overall V - I characteristics of p-n junction

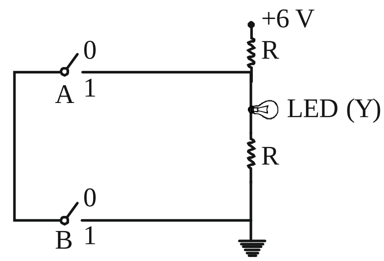
Q.53 In the combination of the following gates the output Y can be written in terms of inputs A and B as **[NEET 2018]**



(A) $\overline{A \cdot B} + A \cdot B$ (B) $A \cdot \overline{B} + \overline{A} \cdot B$
(C) $\overline{A \cdot B}$ (D) $\overline{A + B}$

Q.54 For a p-type semiconductor, which of the following statements is true ? **[NEET 2019]**
(A) Electrons are the majority carriers and trivalent atoms are the dopants.
(B) Holes are the majority carriers and trivalent atoms are the dopants.
(C) Holes are the majority carriers and pentavalent atoms are the dopants.
(D) Electrons are the majority carriers and pentavalent atoms are the dopants.

Q.55 The correct Boolean operation represented by the circuit diagram drawn is : **[NEET 2019]**



(A) AND (B) OR
(C) NAND (D) NOR

ANSWER KEY

EXERCISE - 1

Q	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	C	A	D	D	C	B	D	B	C	A	A	A	D	D	D	B	A	C	B	D	D	C	B	A	D
Q	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
A	C	B	B	C	A	C	A	D	D	B	B	B	D	A	D	B	A	C	C	C	A	A	A	B	C
Q	51	52	53	54	55	56	57	58	59																
A	A	D	B	A	B	A	B	B	D																

EXERCISE - 2

Q	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	A	B	D	C	A	B	A	B	B	B	D	A	D	C	C	B	A	B	B	C	A	B	D	A	A
Q	26	27	28	29	30	31	32	33	34	35	36	37	38												
A	B	D	D	C	B	B	A	B	A	C	D	B	D												

EXERCISE - 3

Q	1	2	3	4	5	6	7
A	2	2	6	24	9	10	50

EXERCISE - 4

Q	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	A	C	C	A	B	A	B	C	D	B	A	C	C	C	A	D	C	D	B	D	D	D	D	C	C
Q	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
A	A	A	D	A	A	B	A	C	B	B	D	D	B	AC	D	C	A	A	B	D	C	D	C	C	A
Q	51	52	53	54	55																				
A	C	C	B	12	40																				

EXERCISE - 5

Q	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	C	A	C	C	D	B	C	C	D	A	D	C	B	C	C	C	C	B	B	A	D	A	B	D	D
Q	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
A	D	D	B	A	C	A	B	B	D	D	A	D	B	D	B	A	B	A	D	B	A	C	B	B	D
Q	51	52	53	54	55																				
A	D	D	B	B	C																				

SEMICONDUCTOR & COMMUNICATION SYSTEMS

TRY IT YOURSELF - 1

(1) **(C).** For P-type semiconductor the doping impurity should be trivalent.

(2) **(C).** Because As is pentavalent impurity.

(3) **(A).** ac $\rightarrow$ Rectifier $\rightarrow$ dc

(4) **(A).** The depletion layer is the region at the junction of a diode which is devoid of charge carriers. Therefore the potential barrier in the depletion layer is due to ions.

(5) **(C).** In n-p-n transistor current flows form base to emitter. Therefore in n-p-n transistor negative charge moves from emitter to base

(6) **(A).** $\beta = \frac{\alpha}{1-\alpha} = \frac{0.95}{1-0.95} = \frac{0.95}{0.05} = 19$

(7) **(C).** Given Current gain of common base $(\alpha) = \frac{I_c}{I_e} = 0.96$.

We know that current gain of common emitter

$$(\beta) = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = \frac{0.96}{0.04} = 24$$

(8) **(D).**

(9) **(A).** The output ac voltage is 2.0 V. So, the ac collector current $i_C = 2.0/2000 = 1.0$ mA.

The signal current through the base is, therefore given by

$i_B = i_C/\beta = 1.0\text{ mA}/100 = 0.010$ mA.

The dc base current has to be $10 \times 0.010 = 0.10$ mA.

$R_B = (V_{BB} - V_{BE})/I_B$.

Assuming $V_{BE} = 0.6$ V,

$R_B = (2.0 \,.\, 0.6)/0.10 = 14\,k\Omega$.

(10) **(B).** The dc collector current $I_C = 100 \times 0.10 = 10$ mA.

TRY IT YOURSELF - 2

(1) **(C).**

(2) **(A).**

(3) For given logic gate $Y = A\overline{B} + \overline{A}B$

Consider lower steps in given wave form as 0 and upper step as 1, we can draw output wave form as

output Y

(4) (B)

(5) (C)

(6) (B)

(7) **(a) OR gate, (b) AND gate**

In fig. (a), $y_1 = \overline{A+B}$ and $Y = \overline{y_1}$

$\therefore \quad Y = \overline{\overline{A+B}} = A+B$ (Boolean algebra)

Clearly fig. (a) represents an OR gate.

in fig. (b), $Y = \overline{y_1 + y_2} = \overline{y_1}.\overline{y_2}$

(Using de Morgan theorem)

But $y_1 = \overline{A}$ and $y_2 = \overline{B}$

$\therefore Y = \overline{y_1}.\overline{y_2} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A.\,B$ which is an AND operation.

Clearly fig. (b) represents an AND gate.

TRY IT YOURSELF - 3

(1) **(B).** FM because modulation index $\propto$ B.W.

(2) **(B).** 10 kHz cannot be radiated (antenna size), 1 GHz and 1000 GHz will penetrate.

(3) **(B).** B.W. of optical fibre ranges from 10^{13} to 10^{15} Hz.

(4) **(A).** Frequency of radiation

$\nu = 200\text{ MHz} = 200 \times 10^6$ Hz

Speed of light, $C = 3 \times 10^8$ m/sec

Wavelength of wave, $\lambda = \frac{C}{\nu} = \frac{3 \times 10^8}{200 \times 10^6} = 1.5\text{m}$

Length of half wave dipole antenna $= \frac{\lambda}{2} = \frac{1.5}{2} = 0.75\text{m}$

(5) **(B).** Let h be the height of a transmission tower.

Population density, $\rho = 1000\text{ km}^{-2} = 1000 \times 10^{-6}\text{ m}^{-2}$

$= 10^{-3}\text{ m}^2$

Now, $d = \sqrt{2Rh}$ (where R is radius of the earth)

Population covered $= \rho\pi d^2 = \rho\pi.2hR$

$\therefore\ 20 \times 10^5 = 10^{-3} \times \frac{22}{7} \times 2 \times h \times 6400 \times 10^3 \ \therefore\ h = 50\text{m}$

(6) **(A).** When carrier is suppressed the percentage saving is

$$P_{saving} = \frac{1}{1+\frac{m^2}{2}} = 66.6\%$$

(7) **(A).** B.W. $= 2 \times f_m = 2 \times 1500 = 3$ kHz.

(8) **(A).** Carrier swing $= \frac{\text{Frequency deviation}}{\text{Modulating frequency}} = \frac{50}{7} = 7.143$

CHAPTER- 8 : SEMICONDUCTOR & COMMUNICATION SYSTEMS

EXERCISE-1

(1)	(C)	**(2)**	(A)	**(3)**	(D)	**(4)**	(D)
(5)	(C)	**(6)**	(B)	**(7)**	(D)	**(8)**	(B)
(9)	(C)	**(10)**	(A)	**(11)**	(A)	**(12)**	(A)
(13)	(D)	**(14)**	(D)	**(15)**	(D)		

(16) **(B).** In forward biasing the diffusion current increases and drift current remains constant so not current is due to the diffusion.
In reverse biasing diffusion becomes more difficult so net current (very small) is due to the drift.

(17) **(A).** During the formation of p-n junction, and due to the concentration gradient across p- and n-sides, holes diffuse from p-side to n-side ($p \to n$) and electrons diffuse from n-side to p-side ($n \to p$).
This motion of charge carriers gives rise to diffusion current across the junction. Electrons drift to give current.

(18) **(C).** After a large reverse voltage is PN-junction diode, a huge current flows in the reverse direction suddenly. This is called Breakdown of PN-junction diode.

(19) **(B).** When reverse bias is increased, the electric field at the junction also increases. At some stage the electric field breaks the covalent bond, thus the large number of charge carriers are generated. This is called Zener breakdown.

(20) **(D).** Barrier potential of a P-N junction diode does not depend on Diode design.

(21) **(D).** Arsenic has five valence electrons, so it is a donor impurity. Hence X becomes
N-type semiconductor. Indium has only three outer electrons, so it is an acceptor impurity. Hence Y becomes P-type semiconductor. Also N (i.e. X) is connected to positive terminal of battery and P(i.e. Y) is connected to negative terminal of battery so PN-junction is reverse biased.

(22) **(C).** In depletion zone, internal electric field is directed from N to P side which opposes diffusion of majority charge carriers.

(23) **(B).** In unbiased condition of PN-junction, depletion region is generated which stops the movement of charge carriers.

(24) **(A).** In the given condition, diode is in reverse biasing so it acts as open circuit. Hence potential difference between A and B is 6V

(25) **(D).** For full wave rectifier

$$\eta = \frac{81.2}{1+\frac{r_f}{R_L}} \Rightarrow n_{max} = 81.2\% \quad (r_f << R_L)$$

(26) **(C).** In a full wave rectifiers, input ac current has a frequency 'ν'. The output frequency of current is 2ν

(27) **(B).** For half wave rectifier, if peak value of output is V_m then its average value on D.C. value (both are same)

$$= \frac{V_m}{\pi}$$

(28) **(B).** As the output voltage obtained in a half wave rectifier circuit has a single variation in one cycle of ac voltage, hence the fundamental frequency in the ripple of output voltage would be = 50 Hz.

(29) **(C).** For a wide range of values of load resistance, the current in the zener diode may change but the voltage across it remains unaffected. Thus the output voltage across the zener diode is a regulated voltage.

(30) **(A).** The maximum permissible current is

$$I_{Z_{max}} = \frac{P}{V_Z} = \frac{364 \times 10^{-3}}{9.1} = 40 \text{ mA}$$

(31) **(C).** Semiconductor diodes in which charge carriers are generated by photons (photo-excitation) are called opto electronic devices. Opto elelctronic devices are

(i) Photodiodes used for detecting optical signal (photo detectors). Used near automatic doors.

(ii) Light Emitting Diodes (LED) which convert electrical energy into light.

(iii) Photovoltaic devices which convert optical radiation into electricity (solar cells).

(32) **(A).** GaAs is better (in spite of its higher band gap) than Si because of its relatively higher absorption coefficient.

(33) **(D).** Light emitting diodes emits visible region of electromagnetic spectrum under applied forward bias.

(34) **(D).** The emitter base junction is forward biased while collector base junction is reversed biased.

(35) **(B).** Because emitter (N) is common to both, base (P) and collector (N).

(36) **(B).** Emitter is heavily doped.

(37) **(B).** As we know $i_E = i_C + i_B$

$$\frac{i_E}{i_C} = 1 + \frac{i_B}{i_C} \Rightarrow \frac{1}{\alpha} = 1 + \frac{1}{\beta} \Rightarrow \beta = \frac{\alpha}{1-\alpha}$$

(38) **(D).** For CE configuration voltage gain $= \beta \times R_L / R_i$

$$\text{Power gain} = \beta^2 \times R_L / R_i \;\Rightarrow\; \frac{\text{Power gain}}{\text{Voltage gain}} = \beta$$

(39) **(A).** For transistor as an amplifier, emitter-Base has to be in forward bias and collector base has to be in reverse bias.

(40) **(D).** Doping level order : Emitter > Collector > Base

(41) **(B).** $i_E = i_B + i_C$
As some electrons combine with holes at base, i.e. $i_B \neq 0$, so $i_E > i_C$

(42) **(A).** In the schematic symbols used for representing n-p-n transistors. The arrowhead from base to emitter. shows the direction of conventional current in the transistor.

(43) **(C).** For a transistor amplifier, the voltage gain is low at high and low frequencies and constant at mid frequencies.

(44) **(C).** The reciprocal of the slope of the linear part of the output characteristic gives the values of r_0. The output resistance of the transistor is mainly controlled by the bias of the base-collector junction.

(45) **(C).** I_B does not depends on V_{CE}. So, when V_{CE} is increased, I_B remains constant increase in V_{CE} appears as increase in V_{CB}. So, effect on I_B is negligible.

(46) **(A).** Voltage gain= current gain × resistance gain

$$= \beta \times \frac{\text{output resistance}}{\text{input resistance}} = \beta \times \frac{R_L}{r}$$

Power gain = voltage gain × current gain

$$= \beta \frac{R_L}{r} \times \beta = \beta^2 \frac{R_L}{r}$$

(47) **(A).** **Input resistance (r_i) :** Ratio of change in base emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). This is dynamic (ac resistance) and as can be seen from the input characteristic, its value varies with the operating current in the transistor.

$$r = \left[\frac{\Delta V_{BE}}{\Delta I_B}\right]_{V_{CE}}$$

(48) **(A).** The given symbol is of 'AND' gate.

(49) **(B).** It is the symbol of 'NOR' gate.

(50) **(C).** If inputs are A and B then output for NAND gate is

$$Y = \overline{AB}$$

$\Rightarrow$ If $A = B = 1$, $Y = \overline{1.1} = \overline{1} = 0$

(51) **(A).** The given symbol is of NAND gate.

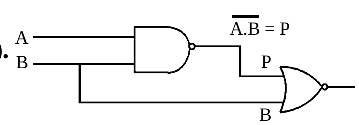
(52) **(D).** 'NOR' gates are considered as universal gates, because all the gates like AND, OR, NOT can be obtained by using only NOR gates.

(53) **(B).** The output of OR gate is $Y = A + B$.

(54) **(A).** $A = 1, B = 1$; Hence $Y = 0$
$A = 0, B = 0$; Hence $Y = 1$
$A = 0, B = 1$; Hence $Y = 1$
$A = 1, B = 0$; Hence $Y = 1$
$A = 1, B = 1$; Hence $Y = 0$
$A = 0, B = 0$; Hence $Y = 1$
$A = 0, B = 1$; Hence $Y = 1$
This input and output shows NAND gate

(55) **(B).** In OR gate, output exists when either of inputs exist.

(56) **(A).**



$$Y = \overline{P + B} = \overline{P}.\overline{B} = \overline{\overline{A.B}}.\overline{B} = A.(B.\overline{B}) = A.0 = 0$$

(57) **(B).** AND gate

(58) **(B).** Diode D_1 is reverse biased as p side is connected to negative potential and n side to ground.
Diode D_2 is forward biased as p side is grounded and n side is at negative potential.

(59) **(D).** Light pulse produce digital signals.

EXERCISE-2

(1) **(A).** In forward biased PN-junction, external voltage decreases the potential barrier, so current is maximum. While in reversed biased PN-junction, external voltage increases the potential barrier, so the current is very small.

(2) **(B).** In reverse biasing, width of depletion layer increases.

(3) **(D).** Given $i_C = \frac{80}{100} \times i_E \Rightarrow 24 = \frac{80}{100} \times i_E$

$\Rightarrow i_E = 30\text{ mA}$

By using $i_E = i_B + i_C \Rightarrow i_B = 30 - 24 = 6\text{ mA}$.

(4) **(C).** $\alpha = \frac{i_C}{i_E} = 0.96$ and $i_E = 7.2\text{ mA}$

$\Rightarrow i_C = 0.96 \times i_E = 0.96 \times 7.2 = 6.91\text{ mA}$

$\therefore i_E = i_C + i_B \Rightarrow 7.2 = 6.91 + i_B$

$\Rightarrow i_B = 0.29\text{ mA}$.

(5) **(A).** Current gain $\beta = \frac{\Delta i_C}{\Delta i_B}$

$\Rightarrow \Delta i_C = \beta \times \Delta i_B = 80 \times 250\ \mu A$.

(6) **(B).** $\alpha = \frac{\beta}{1+\beta} = \frac{99}{1+99} = 0.99$.

(7) **(A).** $\Delta V_C = 0.5\text{ V}$; $\Delta i_C = 0.05 \times 10^{-3}\text{A}$
Output resistance is given by

$$R_{out} = \frac{\Delta V_C}{\Delta i_C} = \frac{0.5}{0.05 \times 10^{-3}} = 10^4\,\Omega = 10\text{ k}\Omega.$$

(8) **(B).** Current gain

$$\beta = \frac{\Delta i_C}{\Delta i_B} \Rightarrow \Delta i_B = \frac{1 \times 10^{-3}}{100} = 10^{-5}\text{A} = 0.01\text{mA}.$$

By using $\Delta i_E = \Delta i_B + \Delta i_C$

$\Rightarrow \Delta i_E = 0.01 + 1 = 1.01\text{mA}$.

(9) **(B).** For 'AND' gate, if output is 1 then both inputs must be 1.

(10) **(B).** **Output resistance (r_0) :** Ratio of change in collector-emitter voltage (ΔV_{CE})to the change in collector current (ΔI_C) at a constant base current I_B,

$$r_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$$

(11) **(D).** For 'NAND' gate $C = \overline{A.B}$

i.e. $\overline{0.0} = \overline{0} = 1$, $\overline{0.1} = \overline{0} = 1$

$\overline{1.0} = \overline{0} = 1$, $\overline{1.1} = \overline{1} = 0$

(12) **(A).** In CE mode, Input current = I_B
Output current = I_C

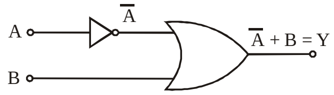
From $\beta = \frac{I_C}{I_B}, \frac{3.5mA}{I_B} = \frac{\alpha}{1-\alpha} = 49$

$\Rightarrow \; I_B = \frac{3.5mA}{49} = 0.071\, mA$

(13) **(D).** $\alpha = 0.9\,;\; \beta = \frac{\alpha}{1-\alpha} = \frac{0.9}{1-0.9} = 9 = \frac{\Delta i_C}{\Delta i_B}$

$\Rightarrow \Delta i_C = 9\,\Delta i_B = 9 \times 4\, mA = 36mA$

(14) **(C).**



(15) **(C).** Current will flow when diode is forward biased.

(16) **(B).** If all the donor states in n-type semiconductor are filled, the number of electrons in donor states will increase.
Due to it, the charge density in donor states will become more than one.

(17) **(A).** A vibrating tuning fork produce analog signals which is a continuous set of values.

(18) **(B).** $n_e = 6 \times 10^{18}\, m^{-3}$
Volume = 1 cm × cm × l mm = $10^{-7}\, m^3$
Number of holes = Number of electrons
$= n_e \times V = 6 \times 10^{18} \times 10^{-7} = 6 \times 10^{11}$

(19) **(B).** Let V be the potential difference between A and B, then $V - 0.3 = (5+5) \times 10^3 \times (0.2 \times 10^{-3}) = 2$
or $V = 2 + 0.3 = 2.3\, V$

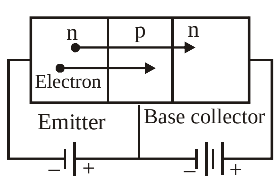
(20) **(C).** For forward biasing,
$\Delta V = 2.4 - 2.0 = 0.4\, V$
$\Delta I = 80 - 60 = 20\, mA$

$\therefore \; r_{fb} = \frac{\Delta V}{\Delta I} = \frac{0.4}{20 \times 10^{-3}} = 20\Omega$

For reverse biasing, $\Delta V = -2 - 0 = -2\, V$
$\Delta I = -0.25 - 0 = -0.25\, \mu A$

$r_{rb} = \frac{-2}{-0.25 \times 10^{-6}} = 8 \times 10^6 \Omega$

(21) **(A).**



(22) **(B).** When a transistor is used as an amplifier with positive feed back, it works as an oscillator.

(23) **(D).** The conductivity of a semiconductor increases with increase in temperature because number density of current carriers increases, relaxation time decreases but effect of decrease in relaxation time is much less than increase in number density.

(24) **(A).** Donor energy level is slightly less than energy level lowest to conduction band.

(25) **(A).** $n_e n_h = n_i^2$ or $n_h = \frac{n_i^2}{n_e}$

$n_i = 1.5 \times 10^{16}\, m^{-3}, n_e = 5 \times 10^{22}\, m^{-3}$

$\therefore \; n_h = \frac{(1.5 \times 10^{16})^2}{5 \times 10^{22}} = \frac{2.25 \times 10^{32}}{5 \times 10^{22}} = 4.5 \times 10^9\, m^{-3}$

(26) **(B).** If input frequency is decreased then more part of AC component goes across R_L.

(27) **(D).** $E_g = 2eV$. Wavelength of radiation corresponding to this energy is $\lambda = \frac{hc}{E_g} = \frac{1240\text{ eV nm}}{2\text{ eV}} = 620\text{ nm}$

Frequency, $\nu = \frac{c}{\lambda} = \frac{3 \times 10^8\, ms^{-1}}{620 \times 10^{-9}\, m} = 5 \times 10^{14}\, Hz$

(28) **(D).** Diffusion is like opening of a scent bottle in a room. Scent particles spread from region of higher to lower concentration.

(29) **(C).** In an unbiased p-n junction, the diffusion of charge carriers across the junction takes place from higher concentration to lower concentration.

(30) **(B).** $V_B = i_B R_B \Rightarrow R_B = \frac{9}{35 \times 10^{-6}} = 257\, k\Omega$

(31) **(B).** Energy of incident photon,

$E = \frac{hc}{\lambda} = \frac{6.6 \times 10^{-34} \times 3 \times 10^8}{6 \times 10^{-7} \times 1.6 \times 10^{-19}} = 2.06\, eV$

The incident radiation can be detected by a photo diode if energy of incident photon is greater than the band gap. As, D_2 = 2eV
$\therefore$ D_2 will detect these radiations.

(32) **(A).** A photodetector detects any change in intensity of light by changing either potential difference across it or by changing current through it.

(33) **(B).** Since, $\beta = \frac{\alpha}{1-\alpha} \;\therefore\; \alpha\beta = \frac{\alpha^2}{1-\alpha}$ .... (1)

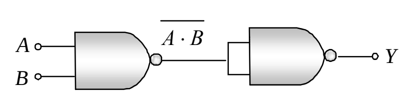
$\beta - \alpha = \frac{\alpha}{1-\alpha} - \alpha$ or $\beta - \alpha = \frac{\alpha^2}{1-\alpha}$ ... (2)

$\therefore \; \frac{\beta - \alpha}{\alpha\beta} = \left(\frac{\alpha^2}{1-\alpha}\right)\left(\frac{1-\alpha}{\alpha^2}\right) = 1$

(34) (A) **(35)** (C) **(36)** (D)
(37) (B) **(38)** (D)

EXERCISE-3

(1) **2.** Two 'NAND' gates are required as follows



$Y = \overline{\overline{AB}.\overline{AB}} = AB$

(2) **2.** Current flow is possible and $i=\frac{V}{R}=\frac{(4-1)}{300}=10^{-2}\,A$

(3) **6.** $E=\frac{V}{d}=\frac{0.5}{5\times10^{-7}}=10^{6}\ V/m$.

(4) **24.** $\beta=\frac{\alpha}{1-\alpha}=\frac{0.96}{1-0.96}=24.$

(5) Voltage gain = β × Resistance gain

$$\beta=\frac{\alpha}{1-\alpha}=\frac{0.99}{(1-0.99)}=99$$

Resistance gain $=\frac{10\times10^{3}}{10^{3}}=10$

⇒ Voltage gain = 99 × 10 = 990.

(6) **10.** Given : Total BW = 100 kHz, $f_{a\,max}$ = 5 kHz
Any station being modulated by a 5 kHz signal will produce an upper-side frequency 5 kHz above its carrier and a lower-side frequency 5 kHz below its carrier, thereby requiring a bandwidth of 10 kHz. Thus,
Number of stations accommodated

$$=\frac{\text{Total BW}}{\text{BW per station}}=\frac{100\times10^{3}}{10\times10^{3}}$$

Number of stations accommodated = 10 stations.

(7) **50.** Modulating signal amplitude $E_m = 30$
Carrier wave amplitude $E_C = 60$
Modulation index , $m_v=\frac{E_m}{E_C}\times100=\frac{30}{60}\times100=50\%$

EXERCISE-4

(1) **(A).** As temperature increases, no. of free electrons also increases. So conductivity increases.

(2) **(C).** At '0K' temperature there is no free electron so it behaves like insulator.

(3) **(C).** Insulators

(4) **(A).** Dopping in emitter is maximum because it is used to produce free change carriers.

(5) **(B).** Electric field is maximum

(6) **(A).** As temperature increases, no. of free electron increases so resistance also vary.

(7) **(B).** When temperature decreases, resistance of metal (conductor) decreases and resistance of semiconductor (germanium) increases.

(8) **(C).** When npn transistor is used as an amplifier electron move emitter to base and then base to collector.

(9) **(D).** When temperature decreases, resistance of metal (conductor) decreases and resistance of semiconductor (germanium) increases.

(10) **(B).** Pauli's exclusion principle

(11) **(A).** When p-n junction is forward biased then applied electric field and electric field of depletion layer are in opposite direction.

(12) **(C).** $\underset{(ev)}{\Delta E}=\frac{12420\times10^{-10}}{\lambda}=\frac{12420\times10^{-10}}{2480\times10^{-9}}=0.5eV$

(13) **(C).** Frequency of ripple in full wave rectifier = 2 × input frequency = 2 × 50 = 100 Hz.

(14) **(C).** Zero

(15) **(A).** $\frac{I_e}{I_h}=\frac{n_e eAV_e}{n_h eAV_h}$; $\frac{7}{4}=\frac{7}{5}\times\frac{V_e}{V_h}$; $\frac{V_e}{V_h}=\frac{5}{4}$

(16) **(D).** If it is not transparent to visible light then forbidden energy gap should be order of 1.5eV to 3eV so it is semiconductor and bond is covalent.

(17) **(C).** $\beta=\frac{I_C}{I_B}=\frac{5.488mA}{I_B}$;

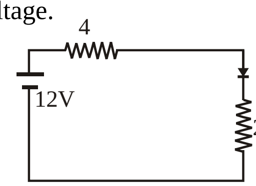
$I_e = I_C + I_B$; $5.6 = 5.488 + I_B$; $I_B = 0.112$ mA

$\beta=\frac{5.488}{0.112}=49$

(18) **(D).** E_C and E_V increase, but E_g decreases.

(19) **(B).** In reverse biasing P should be at lower voltage and n should be at higher voltage.

(20) **(D).** D_1 is in reverse biasing, so current will not flow through D_1.



$I=\frac{12}{6}=2A$

(21) **(D).** When applied voltage is '–5V' current will not flow through junction so output voltage is zero, but when applied voltage is '+5V' current will flow through junction and output voltage is '+5V'.

(22) **(D).** Forbidden energy gap is small in Si and Ge but big in case of carbon.

(23) **(D).** No conduction is found between P and Q]
So P and Q are emitter or collector. So R is base.

(24) **(C).** When potential is applied on A or on B or on both then one or both junction are forward biased, so cut potential drop B on resistor so 'C' have potential equals to applied at A, B or both, so it is OR gate.

(25) **(C).** Current will flow when diode is forward biased.

(26) **(A).**

(27) **(A).** Truth table for given combination is

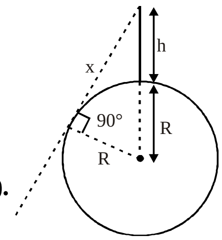
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

This comes out to be truth table of OR gate.

(28) **(D).** The state of ionosphere varies from hour to hour, day to day and season to season.

(29) **(A).**

(30) (A).



$r = R + h \cong R$

$x = \sqrt{(R+h)^2 - R^2} = \sqrt{h^2 + 2hR}$

$x^2 = 25000 + 2 \times 500 \times 6.4 \times 100000$

$= 25000 + (64 \times 100000000) = 10^4\,(640025)$

$x^2 = 10^4 \times (640025)\,;\ x = 8 \times 10^4\,m = 80\,km$

(31) (B). $\tau = RC = 100 \times 10^3 \times 250 \times 10^{-12}$ sec

$= 2.5 \times 10^7 \times 10^{-12}$ sec $= 2.5 \times 10^{-5}$ sec

The higher frequency which can be detected with tolerable distortion is

$$f = \frac{1}{2\pi m_a RC} = \frac{1}{2\pi \times 0.6 \times 2.5 \times 10^{-5}}\,Hz$$

$$= \frac{100 \times 10^4}{25 \times 1.2\pi}\,Hz = \frac{4}{1.2\pi} \times 10^{-4} = 10.61\,KHz$$

This condition is obtained by applying the condition that rate of decay of capacitor voltage must be equal or less then the rate of decay modulated singnal voltage for proper detection of mdoulated signal.

(32) (A). For same value of current higher value of voltage is required for higher frequency.

(33) (C). For forward Bias, p-side must be at higher potential than n-side.

(34) (B). Frequencies of resultant signal are

$_e + f_m$, f_e and $f_e - f_m$

(2000 + 5) kHz, 2000 kHz, (2000 – 5) kHz,

2005 kHz, 2000 kHz, 1995 kHz

(35) (B). Resistance of conductor increases and resistance of a semiconductor decreases with increase in temperature.

(36) (D).

(37) (D).

(38) (B). Since x = 1 if either a, b, c or d = 1

$x = a \cup b \cup c \cup d$. The gate is OR.

(39) (AC). We know that $\beta = \dfrac{\alpha}{1-\alpha}$

So, $\dfrac{1}{\alpha} = \dfrac{1}{\beta} + 1$ and $\alpha = \dfrac{\beta}{1+\beta}$ are correct

(40) (D). The frequencies in amplitude modulated wave is between $\omega_c - \omega_m$ and $\omega_c + \omega_m$.

(41) (C). $v_0 = \Delta(V_{cc} - i_c R_c) = -\Delta i_c R_c$

$v_i = \Delta(v_{BE} + i_B R_B) = \Delta i_B R_B$

$$A_v = \frac{v_0}{v_i} = -\frac{\Delta i_c}{\Delta i_B}\frac{R_c}{R_B} = -\beta\frac{R_c}{R_B}$$

"–ve" sign indicates output is exactly out of phase i.e. phase difference = 180°.

(42) (A). Voltage across Si diode in forward bias is 0.7 volts. Hence voltage across 200 Ω resister is 3 – 0.7 = 2.3V

$\therefore\ I = \dfrac{2.3}{200} = 11.5\,mA$

(43) (A). Overall bandwidth use for transmission = 10% of v_C

Number of telephonic channel

$$= \frac{\text{Total bandwidth}}{\text{Channel bandwidth}} = \frac{\frac{10}{100} \times 10 \times 10^9}{5 \times 10^3} = 2 \times 10^5$$

(44) (B). $j = \sigma E = nev_d$; $\sigma = ne\dfrac{v_d}{E} = ne\mu$

$$\frac{1}{\sigma} = \rho = \frac{1}{n_e e\mu_e} = \frac{1}{10^{19} \times 1.6 \times 10^{-19} \times 1.6} = 0.4\,\Omega\,m$$

(45) (D). $f = \dfrac{3 \times 10^8}{8 \times 10^{-7}} = \dfrac{30}{8} \times 10^{14}\,Hz = 3.75 \times 10^{14}\,Hz$

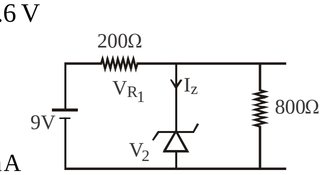
1% of f = 0.0375×10^{14} Hz

$= 3.75 \times 10^{12}\,Hz = 3.75 \times 10^6$ MHz

Number of channels $= \dfrac{3.75 \times 10^6}{6} = 6.25 \times 10^5$

(46) (C). $9 = V_Z + V_{R_1}$; $V_Z = 5.6$ V

$V_{R_1} = 9 - 5.6 = 3.4$

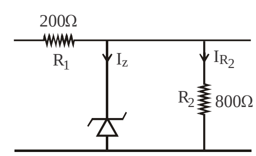


$I_{R_1} = \dfrac{V_{R_1}}{R} = \dfrac{3.4}{200} = 17$ mA

$V_Z = V_{R_2} = I_{R_2}(R_2)$

$\dfrac{5.6}{800} = I_{R_2}$; $I_{R_2} = 7mA$

$I_Z = (17 - 7)\,mA = 10\,mA$



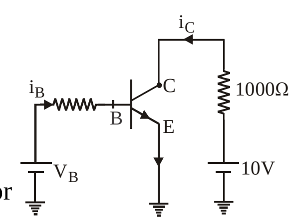
(47) (D). To minimise attenuation, wavelength of carrier waves is close to 1500 nm.

(48) (C). At saturation state,

V_{CE} becomes zero

$i_c = \dfrac{10V}{1000\Omega} = 10mA$

Now current gain factor



$\beta = \dfrac{i_C}{i_B}$; $i_B = \dfrac{10mA}{250} = 40\mu A$

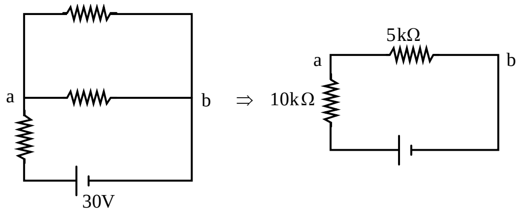
(49) (C). Range $= \sqrt{2Rh_T} + \sqrt{2Rh_R}$

$50 \times 10^3 = \sqrt{2 \times 6400 \times 10^3 \times h_T} + \sqrt{2 \times 6400 \times 10^3 \times 70}$

By solving $h_T = 32$ m

(50) (A). A logic gate is reversible if we can recover input data from the output. eg. NOT gate.

(51) (C).



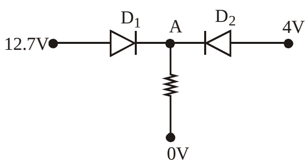
Diode is in forward bias, so it will behave as simple wire so, $V_{ab} = \frac{30}{5+10} \times 5 = 10V$

(52) (C).

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

(53) (B). $Y = \overline{\overline{AB} \cdot A} = \overline{\overline{AB}} + \bar{A} = 0 + 0 = 0$

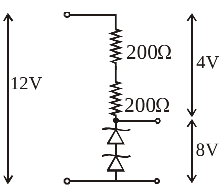
(54) 12.00



Diode D_1 is forward biased and D_2 is reverse biased.

$\therefore \quad V_A = 12.7 - 0.7 = 12V.$

(55) 40.00



Current in circuit $= \frac{4}{400} = \frac{1}{100} A$

So power dissipated in each diode = VI

$4 \times \frac{1}{100} W = 40$ mW

EXERCISE-5

(1) (C).

(A) In case of conductors either the conduction and valance band overlap or conduction band is partially filled.

(B) Insulators have energy gap of 5eV to 10eV.

(C) Resistivity (opposite of conductivity) decreases with increase in temperature.

(D) With increase in temperature more and more electrons jump to the conduction band. So, conductivity increases.

(2) (A). Due to strong electronegativity of carbon.

(3) (C). Number of donors is more because electron from –ve terminal of the cell pushes (enters) the n side and decreases the number of uncompensated pentavalent ion due to which potential barrier is reduced. The neutralised pentavalent atom are again in position to donate electrons.

(4) (C). At a certain reverse bias voltage, zener diode allows current to flow through it and hence maintains the voltage supplied to any load. Hence it is used for stabilisation.

(5) (D). On the basis of given graph following table is possible

A	B	C
0	0	0
1	1	1
0	1	0
1	0	0

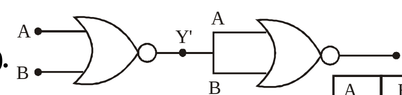
It is the truth table of AND gate.

(6) (B). $\Delta I_B = +50\mu A,\ \Delta I_C = 5 \times 10^{-3} A$

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{5 \times 10^{-3}}{50 \times 10^{-6}} = \frac{5 \times 1000}{50} = 100$$

(7) (C). In forward biasing of a diode, the emitter should be at a higher potential. Here, only in option (C) emitter is at higher potential.

(8) (C).



$Y' = \overline{A + B}$

$Y = \overline{\overline{A + B}} = A + B$

Therefore truth table :

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

(9) (D). For a P-type semiconductor, the acceptor energy level, as shown in the diagram, is slightly above the top E_v of the valence band. With very small supply of energy an electron from the valence band can jump to the level E_A and ionise acceptor negatively.

(10) (A). Voltage gain $= \frac{Av}{1 + \beta A_v}$

$$10 = \frac{Av}{1 + (9/100)A_v} \ ; \ A_v = \frac{10}{0.1} = 100$$

(11) (D). NOR gate

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

(12) (C). $2\text{ eV} = h\nu \ \therefore \ \nu = \frac{2eV}{h}$

$$\nu = \frac{2 \times 1.6 \times 10^{-19}}{6.6 \times 10^{-34}} \approx 5 \times 10^{14} Hz$$

(13) (B). (iv), (ii), (i)

(14) (C). $\lambda_{max} = \frac{hc}{E} = \frac{6.6 \times 10^{-34} \times 3 \times 10^8}{2.5 \times 1.6 \times 10^{-19}} \simeq 5000 Å$

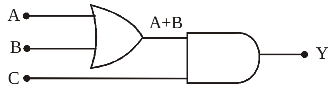
$\lambda < \lambda_{max} = 4000 Å$

(15) **(C).** $\Delta I_E = \Delta I_B + \Delta I_C$; $\beta = \frac{\Delta I_C}{\Delta I_B}$

$\Delta I_C = 5 \times 10^{-3}$ A ; $\Delta I_B = 100 \times 10^{-6}$ A

$\beta = \frac{5}{100} \times 1000 = 50$

(16) **(C).**



The Boolean expression of the given circuit is
$Y = (A + B) . C$
The truth table of the given input signals :

A	B	C	A + B	Y = (A + B).C
0	1	0	1	0
0	0	1	0	0
1	0	1	1	1
1	0	0	1	0

From the truth table output Y = 1,
For the inputs A = 1, B = 0, C = 1

(17) **(C).** Voltage gain = 50
Input resistance, $R_i = 100\Omega$
Output resistance, $R_0 = 200\Omega$

Resistance gain = $\frac{R_0}{R_i} = \frac{200\Omega}{100\Omega} = 2$

Power gain = $\frac{(\text{Voltage gain})^2}{(\text{Resistance gain})} = \frac{50 \times 50}{2} = 1250$

(18) **(B).** In a n-type semiconductors, electrons are majority carriers and holes are minority carriers.

(19) **(B).** The device that can act as a complete circuit is integrated circuit (1C).

(20) **(A).** (ii), (iv) and (iii)

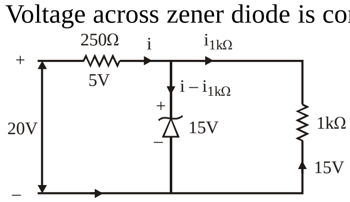
(21) **(D).** Addition of antimony will make it an N-type semiconductor.

(22) **(A).** In forward biasing of the p-n junction the positive terminal of the battery in connected to p-side and the depletion region becomes thin.

(23) **(B).** Only in (a) and (c)
Diodes are forward biased. As p-type should be higher potential & n-type at lower potential.

(24) **(D).** $n_i^2 = n_e n_h$
$(1.5 \times 10^{16})^2 = n_e (4.5 \times 10^{22})$
$n_e = 0.5 \times 10^{10}$; $n_e = 5 \times 10^9$
$n_h = 4.5 \times 10^{22}$; $n_h >> n_e$
Semiconductor is p-type and $n_e = 5 \times 10^9\ m^{-3}$.

(25) **(D).** Voltage across zener diode is constant



$(i)_{1k\Omega} = \frac{15 \text{ volt}}{1k\Omega} = 15mA$

$(i)_{250\Omega} = \frac{(20-15)\ V}{250\Omega} = \frac{5V}{250\Omega} = \frac{20}{1000} A = 20mA$

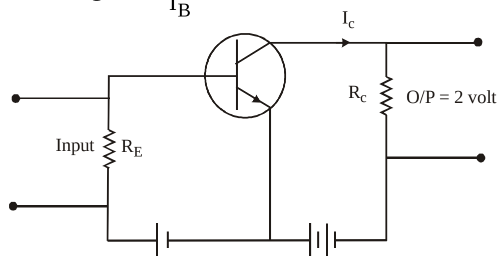
$\therefore\ (i)_{\text{zener diode}} = (20 - 15) = 5mA$

(26) **(D).** Here D_1 is in forward bias and D_2 is in reverse bias

so $I = \frac{V}{R} = \frac{5}{10} = \frac{1}{2}$ amp.

(27) **(D).** $V_o = I_C R_C = 2$; $I_C = \frac{2}{2 \times 10^3} = 10^{-3}$ amp

Current gain = $\frac{I_C}{I_B} = 100$



$I_B = \frac{I_C}{100} = \frac{10^{-3}}{100} = 10^{-5}$ amp.

$V_i = R_B I_B = 1 \times 10^3 \times 10^{-5} = 10^{-2}$ volt = 10mV

(28) **(B).** I : Cutoff region, II : Active region
III : Saturation region
When the transistor is used in the cutoff or saturation state, it acts as a switch.

(29) **(A).** OR gate :

A	0	1	1	0
B	0	0	1	1
C	0	1	1	1

(30) **(C).** $^6C = 1s^2, 2s^2\ 2p^2$
$^{14}Si = 1s^2, 2s^2\ 2p^6, 3s^2\ 3p^2$
As they are away from Nucleus, so effect of nucleus is low for Si.

(31) **(A).** Voltage gain = $\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} \times \frac{R_{out}}{R_{in}}$

$= \frac{2 \times 10^{-3}}{40 \times 10^{-6}} \times \frac{4 \times 10^3}{100} = 2 \times 1000 = 2000$

(32) **(B).** When A = 1, B = 0, C = 1 then Y = 1

(33) **(B).** Voltage gain $A_V = \frac{\Delta V_C}{\Delta V_B} = \frac{R_L \Delta I_C}{\Delta V_B} = g_m R_L$

$\frac{A_{V_1}}{A_{V_2}} = \frac{g_{m_1}}{g_{m_2}} \Rightarrow \frac{G}{A_{V_2}} = \frac{0.03}{0.02} \Rightarrow A_{V_2} = \frac{2}{3} G$

(34) **(D).**

A	B	X
0	0	0
1	0	0
0	1	0
1	1	1

; $X = A . B$

(35) **(D).** Holes are minority carriers and pentavalent atoms are dopants.

(36) **(A).** Solar cell $\rightarrow$ Open circuit I = 0, potential V = emf
$\rightarrow$ Short circuit I = I, potential V = 0

(37) **(D).** It depends on all.

(38) **(B).** AND gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(39) **(D).** When applied voltage is '–5V' current will not flow through junction so output voltage is zero, but when applied voltage is '+5V' current will flow through junction and output voltage is '+5V'.

(40) **(B).** Potential difference on R = 3.5 – 0.5 = 3.0 volt

Current in circuit $i = \frac{V}{R} = \frac{3}{100} = 30$ mA

(41) **(A).** Input signal $V_{in} = 2\cos\left(15t + \frac{\pi}{3}\right)$;

Voltage Gain = 150

CE amplifier gives phase difference of π between input and output signals $A_v = \frac{V_0}{V_{in}}$, so $V_0 = A_V V_{in}$

$V_0 = 150 \times 2\cos\left(15t + \frac{\pi}{3} + \pi\right) = 300\cos\left(15t + \frac{4\pi}{3}\right)$

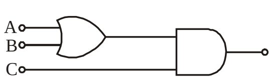
(42) **(B).** $V_A - V_B = IR \Rightarrow 4 + 6 = 10^3 I \Rightarrow I = \frac{10}{10^3} = 10^{-2}$ A

(43) **(A).** $R_L = 800\,\Omega, V_L = 0.8$ V

$\Rightarrow I_C = \frac{V_L}{R_L} = 1$mA ; $R_i = 192\,\Omega$

Current amplification $= \frac{\text{Output current}}{\text{Input current}} = \frac{I_C}{I_B} = 0.96$

$I_B = \frac{1\text{mA}}{0.96}$; $A_v = \frac{V_L}{V_{in}} = \frac{V_L}{I_B R_i} = 4$; $A_p = \frac{I_C^2 R_L}{I_B^2 R_i} = 3.84$

(44) **(D).** 

$= (A + B).C$

To get Y = 1, C should be 1.

(45) **(B).** $R_C = 2k\Omega, V_0 = 4V$

$I_C = \frac{4V}{R_C} = \frac{4V}{2k\Omega} = 2$mA

$\beta = \frac{I_C}{I_B} = 100 \Rightarrow I_B = \frac{I_C}{100} = 2 \times 10^{-5}$ A

$V_{in} = I_B R_i = 2 \times 10^{-5} \times 1\,k\Omega = 20$ mV

(46) **(A).** D_1 is reverse biased ; D_2 is forward biased

$I = \frac{10V}{(2+2)\,\Omega} = 2.5$ A

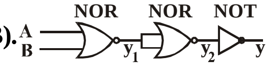
(47) **(C).** Output $Y = \overline{(A \cdot B) \cdot C} = \overline{A} + \overline{B} + \overline{C}$

When A, B, C are 0 $\rightarrow$ Y = 1

When A, B, C are 1 $\rightarrow$ Y = 0

(48) **(B).** $A_V = \beta \frac{R_C}{R_B} = 100 \times \frac{3k\Omega}{2k\Omega} = 150$

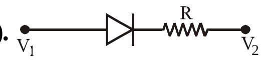
Power gain = $\beta A_V = 100 \times 150 = 15000$

(49) **(B).** 

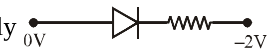
$y_1 = \overline{A + B}$; $y_2 = \overline{y_1 + y_1} = \overline{y}_1 = \overline{\overline{A + B}} = A + B$

$y = \overline{y}_2 = \overline{A + B}$

NOR GATE

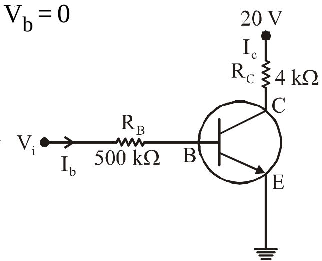
(50) **(D).** 

In forward bias $V_1 > V_2$

Only 

is in forward bias.

(51) **(D).** $V_{BE} = 0$; $V_{CE} = 0$; $V_b = 0$



$I_C = \frac{(20-0)}{4 \times 10^3}$

$I_C = 5 \times 10^{-3} = 5$ mA

$V_i = V_{BE} + I_B R_B$

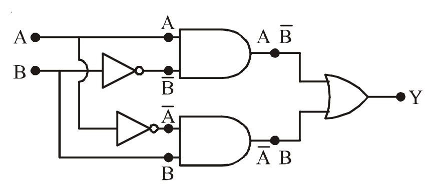
$V_i = 0 + I_B R_B$

$20 = I_B \times 500 \times 10^3$

$I_B = \frac{20}{500 \times 10^3} = 40\,\mu A$; $\beta = \frac{I_C}{I_B} = \frac{25 \times 10^{-3}}{40 \times 10^{-6}} = 125$

(52) **(D).** Due to heating, number of electron-hole pairs will increase, so overall resistance of diode will change. Due to which forward biasing and reversed biasing both are changed.

(53) **(B).** $Y = A \cdot \overline{B} + \overline{A} \cdot B$



(54) **(B).** In p-type semiconductor, an intrinsic semiconductor is doped with trivalent impurities, that creates deficiencies of valence electrons called holes which are majority charge carriers.

(55) **(C).** From the given logic circuit LED will glow, when voltage across LED is high.

Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

This is out put of NAND gate.